Thermal Characteristics of Thin Film VCSELs for Fully Embedded Chip-to-Chip Guided-Wave Optical Interconnection

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Abstract: The thermal characteristics of a thin film VCSEL are studied both theoretically and experimentally. The theoretical analysis of thermal via effects is performed to determine optimized thickness range of VCSEL for the fully embedded structure.

1. Summary

To relieve packaging difficulty, we have developed the fully embedded board-level optical interconnection system which is also depicted in Figure 1 [1-4]. All the optoelectronic components including VCSEL array, PIN-PD array, 45° coupling mirrors and planar polymer waveguides are integrated within the 3-D interconnection layers during the conventional PCB fabrication processes. In this architecture, however, the self-heating effect of the vertical-cavity surface-emitting laser (VCSEL) causes the critical concerns in the system reliability since integrated VCSEL arrays are surrounded by such thermal insulators as optical polymer films and PCB bonding materials (prepreg or pressure-sensitive-adhesive film). Because the operating lifetime of VCSEL decreases exponentially with temperature [5], the thermal management of the embedded VCSEL arrays is one of the prime concerns in the fully embedded optical interconnection system.

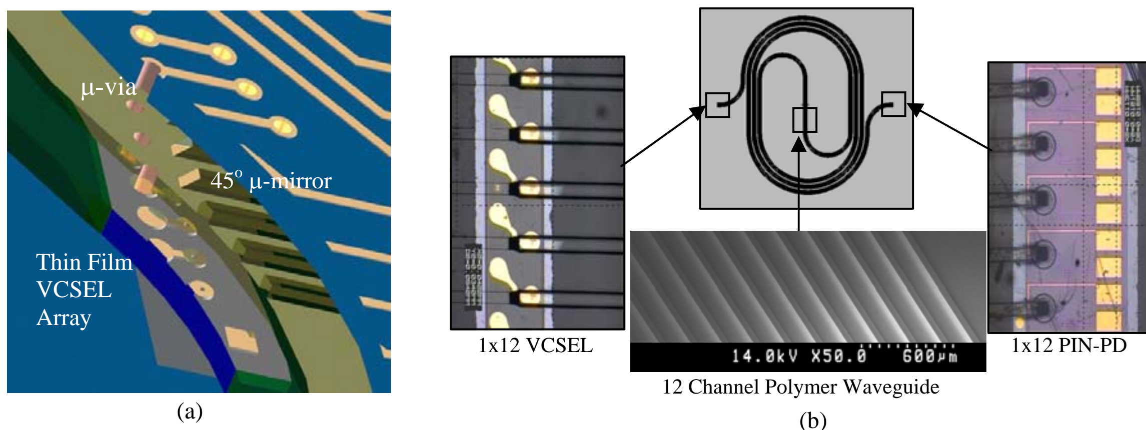

Fig. 1 (a) 3-D cross-section view of an optical layer interposed PCB, (b) 12-channels optical waveguide film layer with integrated thin film VCSEL & PIN-PD arrays.

This paper presents theoretical and experimental studies of the thermal characteristics of the fully embedded thin film VCSEL array which determines the effective thermal via structures. A 12-channel 850 nm oxide-confined VCSEL array with 10 Gbps each is employed as input light sources. The initial 200 μm thick GaAs substrate of VCSEL is removed not only for facilitating the fully embedded integration structure but also for managing VCSEL temperature as previously mentioned. Figure 2(a) and Figure 2(b) show, respectively, a part of VCSEL array before and after the substrate thinning processes.

Due to the self-heating effect of VCSEL, the temperature of active region rises relative to the heat sink. To achieve maximum VCSEL reliability in the fully embedded structure, it is imperative to control VCSEL temperature during operation. The ratio of temperature rise (ΔT) to the net dissipation power (ΔP_{diss}) is defined as the thermal resistance (R_{th}). The thermal resistance is given by

$$R_{th} = \Delta T / \Delta P_{diss} = (\Delta\lambda / \Delta P_{diss}) / (\Delta T / \Delta\lambda)$$

where $\Delta\lambda$ is the wavelength shift. Measured wavelength temperature variation ($\Delta\lambda / \Delta T$) is 0.066 nm/^{o}C. Measured slopes of the wavelength shift as a function of net dissipated power ($\Delta\lambda / \Delta P_{diss}$) for 200 μm, 100 μm, 60 μm, 20 μm and 10 μm thick VCSELs are 188 nm/W, 169 nm/W, 153 nm/W, 144 nm/W and 120 nm/W respectively.

To simulate inside VCSEL temperature rise, the heat source distributions inside VCSEL have to be determined. 2-D thermal-electric coupled field analysis module in ANSYS software is used to calculate the temperature distribution due to the joule heating in the DBRs and the non-radiative recombination in the active region. Calculated and experimentally measured thermal resistances are shown in Figure 3 with ambient temperature set at 25 ^{o}C. Thermal resistance of 10 μm thick VCSEL is 40 % lower than that of 200 μm thick VCSEL. Calculated active region temperatures for 200 μm and 10 μm thick VCSEL are 47.16 ^{o}C and 38.9 ^{o}C, respectively.

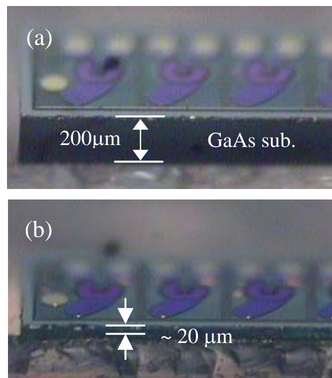

Fig. 2 (a) 200 μm thick VCSEL array (before substrate thinning), (b) 20 μm thick VCSEL array (after substrate thinning)

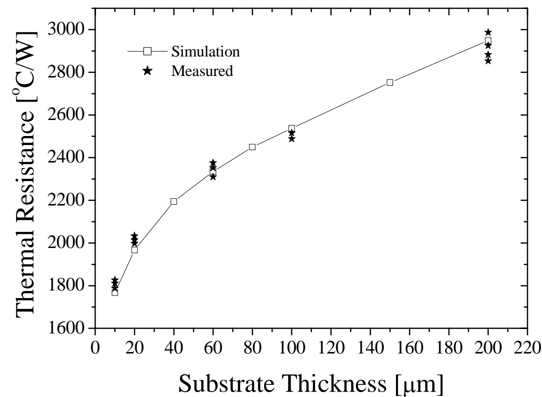

Fig. 3 Simulation and experimental results of thermal resistances as a function of substrate thickness of thin film VCSEL.

Figure 4(a) and Figure 4(b) show simulation results of temperature distribution inside VCSEL with two commonly employed thermal via structures, the closed blind via (copper filled inside via hole-(a)) and the open blind via (30 μm thick copper electroplated inside via hole-(b)), respectively. In this simulation model, we assumed the top of the VCSEL is covered by polymer layer, which are the wave guiding layer as shown in ref [3, 6]. Figure 4(c) shows theoretically determined thermal resistances of the fully embedded thin film VCSEL with different thermal via structures. Following the previous results (Figure 3), the compatible thermal resistance for the fully embedded VCSEL structure should be in the same range of 200 μm thick VCSEL with 25°C substrate cooling condition. Therefore, in this study, the target thermal resistance is determined to be in the range of 2800 ~ 3000 °C/W. In the case of the open blind via structures (straight lines in Figure 4(c)) with an aspect ratio of 1 and 0.5, the effective substrate thickness of thin film VCSEL is estimated in the range of 12 μm ~ 22 μm and 29 μm ~ 46 μm, respectively. Also, in the case of the closed blind via structures (dot lines in Figure 4(c)) with an aspect ratio of 1 and 0.5, the fully embedded structure compatible substrate thickness of VCSEL is in the range of 44 μm ~ 60 μm and 53 μm ~ 72 μm, respectively.

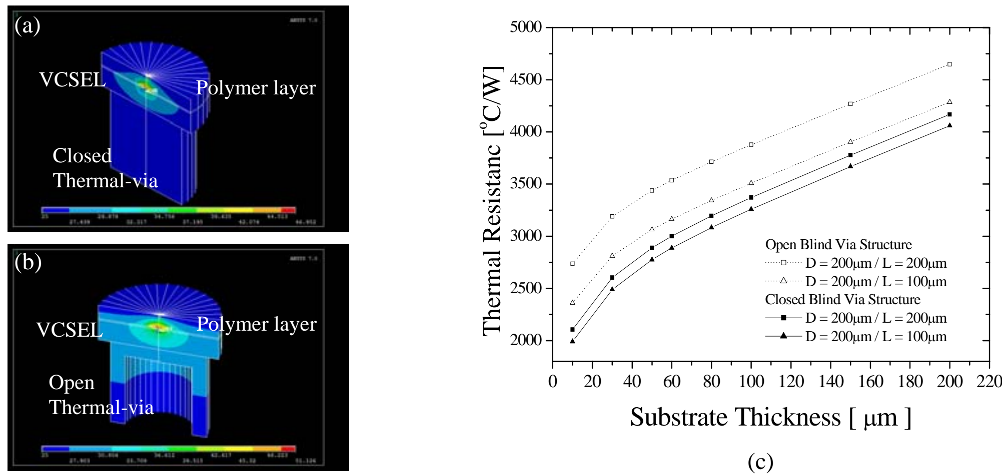

Fig. 4 (a) Thin film VCSEL with a backside closed blind via structure, (b) Thin film VCSEL with a backside open blind via structure, (c) Simulation results of thermal resistance as a function of substrate thickness of thin film VCSEL with different thermal via structures.

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