15-Gb/s Bit-Interleaved Optical Backplane Bus Using Volume Photopolymer Holograms

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***Abstract*—A 15-Gb/s bit-interleaved optical backplane bus interconnection is experimentally demonstrated in a three-board system based on optical backplane using volume photopolymer holograms. During upstream data transferring, bit pulses from each daughter board are superposed to form an interleaved sequence while for downstream data transferring, the data broadcast from the central board are time-division demultiplexed locally at each daughter board, and only the destined bits are stored respectively. In this way, slow electronic chips can be coordinated to generate a high aggregated bandwidth to relieve wiring congestion. Both nonreturn-to-zero and return-to-zero signaling modes based on vertical-cavity surface-emitting laser sources and pulse lasers are independently employed to implement 2.5- and 15-Gb/s operations. This optical bus architecture also provides a secure and reliable data storage method at 850 nm with a bit-error rate better than 10^{-12}.**

***Index Terms*—Bit-interleaved optical backplane (BIOB) bus, reliability, volume photopolymer holograms.**

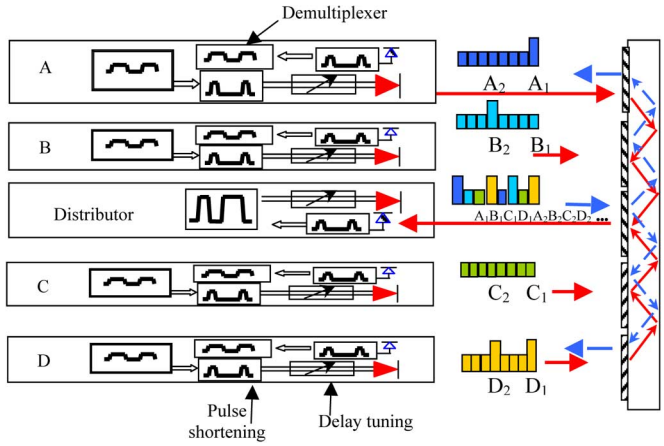

Fig. 1. Conceptual diagram of BIOB bus. Solid arrow: bit-interleaved upward transferring. Dashed arrow: rebroadcasting.

I. Introduction

INTERCONNECT is one of the dominant factors to computer performance [1], especially in high-performance computing (HPC) employing multiple processors. As technologies mature, optical interconnects have been adopted in rack-to-rack HPC systems, because the required product of interconnect distance and bandwidth has surpassed the capacity of electrical interconnects [2]. With the advent and popularity of multicore processors in the HPC market, the demand on transferring data among multiple processing units inside an HPC box will soon reach to a limit that conventional electrical interconnects become inadequate due to the well-known fundamental physical restrictions, including dielectric loss, electromagnetic interference, system weight and size.

One severe performance limiting factor to electrical interconnects is wiring congestion. Because of its bandwidth advantage, the point-to-point topology has replaced the shared-bus topology in the electrical backplane industry. However, wiring congestion is the adverse consequence of this transition, because in order to route all memory modules to the central switch [2], the boards in an HPC system currently tend to use more than 50 wiring layers, and more than 700 signal pins are required for one board edge connector, which needs as large as 100 pounds insertion force to seat [3].

The wiring congestion problem can be greatly mitigated by using an optical bus that allows multiple daughter boards to share a common data channel to transfer information at higher data rate simultaneously, which is demonstrated in this letter. We describe a new optical dual-channel bit-interleaved technology with the purpose to accommodate relatively slow memory modules. With this optical bus architecture, system security and reliability can also be improved by backing up the encoded data in additional memory modules just as a RAID10 mirrors data in a secondary set of disks [4].

II. Optical Bit-Interleaved Technology

The bit-interleaved optical backplane (BIOB) physical layer shown in Fig. 1 consists of two sublayers: an optical layer and a bit-interleaving layer. The optical layer design follows the centralized shared-bus architecture demonstrated with uniform optical fan-out powers [5]. The light beams emitted by the vertical-cavity surface-emitting lasers (VCSELs) and those projected to the photodetectors are surface-normal to the hologram films that function as the coupling devices [6]. The desired diffraction efficiencies for the five slots are 100%, 50%, 50% double, 50%, 100%, respectively, using 20-μm-thick Dupont photopolymer (HRF-600X100-20) with 49-nm 3-dB bandwidth around 850 nm.

The bit-interleaved technology is used by the personal computer industry to allow for more efficient usage of memory accesses. In a system equipped with dual 400-Mb/s double data-rate memory modules, the chipset associated with the CPU reads

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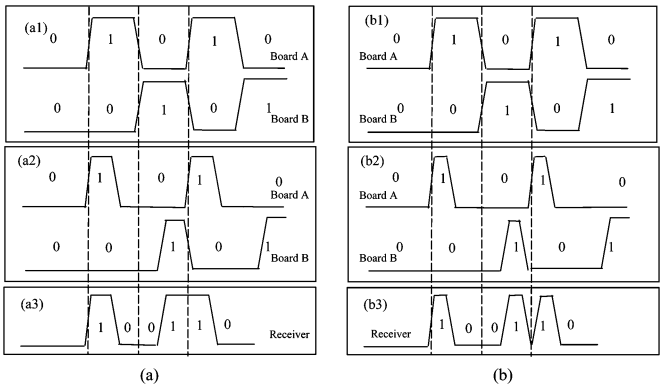

Fig. 2. Illustration of optical bit-interleaving technology: (a) NRZ mode: (a_1) data originated from two boards; (a_2) reshaped and delayed optical bit pulses; (a_3) interleaved optical bit pulses detected by receiver. (b) RZ mode: (b_1) data originated from two boards; (b_2) reshaped and delayed optical bit pulses; (b_3) interleaved optical bit pulses detected by reciever.

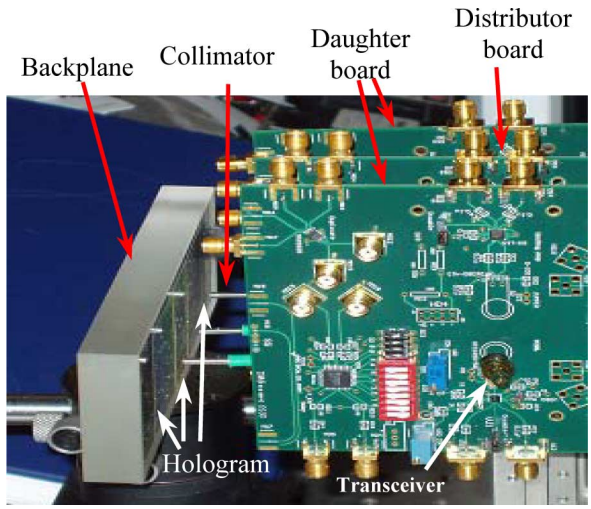

Fig. 3. Experimental setup for BIOB bus.

both memory modules simultaneously, multiplexes the data into an aggregated 800-Mb/s stream, and then feeds it to the CPU. The optical interleaved technology can allow the multiplexing to happen locally to relieve wiring congestion. In BIOB, the signals provided to VCSEL driver are first shortened by the local bit controller. Then the optical bit pulses emitted from VCSEL are delayed by a specific time according to the physical location of the daughter board so that the receiver detects a bit-interleaved optical data stream. Fig. 2(a) illustrates the nonreturn-to-zero (NRZ) mode where the falling and rising edges of two consecutive optical bit pulses overlap. Fig. 2(b) illustrates a relatively conservative operation which is return-to-zero (RZ) mode, since all optical bit pulses must fall to logic zero. When the high-speed data stream from the central board is broadcast, the local demultiplexer collects the destined bits for each daughter board. In this way, wiring congestion can be relieved since all daughter boards share data channel.

A serializer chip (MC10EP445FA, ON Semiconductor) is selected as local bit controller, which could shorten the electrical bit pulses from around 1.6 ns down to 400 ps. Because the optical pulses traveling from different daughter boards to the central receiver possess fixed time delays according to their relative physical locations, we add a tunable time delay chip (SY100EP196 V, Micrel) with resolution better than 5 ps to ensure the total delay difference to be multiples of 400 ps. Since VCSELs emit light even when sending logic 0s, it is necessary to use VCSELs with different wavelengths for different daughter boards so that the beat noise of superposed optical signal at central receiver can be ignored. In the demonstration, peak wavelengths of VCSELs are separated by at least 2 nm, which is greater than 0.4-nm VCSEL linewidth. By sending dc balanced signals from all daughter boards and equalizing the modulation currents, the optical signal arriving at the central photodetector can keep a constant dc level and ac amplitude. A transimpedance amplifier with dc cancellation function will amplify the ac components and forward desired signals to the post amplifiers and CPU.

The BIOB can also be implemented using a pulse laser, which is adopted in optical time-division-multiplexing technology in the telecom industry [7] with electroabsorption modulators [8], [9] for ultrahigh-speed operation.

Because confidential data can be separately distributed into multiple storage devices working in an array format, a benefit of security and enhanced reliability is achieved in addition to the potential to boost system speed and relieve wiring congestion.

III. Experiment

A BIOB system is built following the design in Section II except that there are only two daughter boards as shown in Fig. 3. The VCSEL (SV5637–001 or HFE6390–561, Advanced Optical Components) output power is controlled at around 2 mW with central wavelength around 840 nm. The loss excluding splitting is around 2.7 dB for 850-nm operation and totally there is around 8.7-dB loss for each slot. For 1550 nm, there is around 3-dB additional loss due to low diffraction efficiency. The 3-dB lateral tolerance radius for the photodetector (HFD6380–413, Advanced Optical Components) with collimator lens (from OZ Optics) was approximately 1 mm.

Fig. 4(a) shows 2.5-Gb/s waveforms from the central receiver captured by the oscilloscope (HP83480A) in NRZ mode and Fig. 4(b) shows RZ mode. By adjusting the time delays of the signal and by controlling the modulation current of each VCSEL source from each daughter board, the receiver at the central slot could correctly detect the bit-interleaved optical bit pulses. The NRZ signaling mode operates at a higher data rate than the RZ mode because the rising and falling edges of adjacent optical bit pulses are allowed to overlap. The BIOB operating in the NRZ signaling mode possesses a signal density of 10 Gb/s/cm^2 limited by the packaging of the laser/detector/collimator. Fig. 4(c) illustrates a sequence of interleaved optical bit pulses at 15 Gb/s in RZ mode by using a pulse laser. The worst-case bit-error rate (BER) is estimated to be below 10^{-12} among all modes from measurement of Q-factor.

IV. Discussion

In the BIOB system, critical limiting factors to data rate could come from the following sources: hologram bandwidth, pulse duration, jitter, and power budget. Dispersion of the optical interconnect layer is not an issue for up to 15-Gb/s operation since the 3-dB bandwidth was experimentally verified to be as high as 2.5 THz for 5.08-cm distance [10]. Our calculation shows that

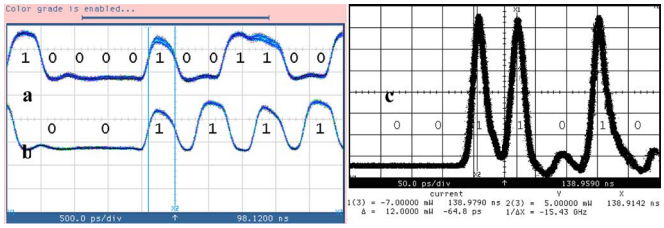

Fig. 4. Interleaved optical bit pulses with BER below 10^{-12} showing a sequence of (a) 10001001100 in 2.5-Gb/s NRZ mode; (b) 1001111 in 1.25-Gb/s RZ mode; (c) 001101 in 15-Gb/s RZ mode.

for 20 boards with 3-cm separation, the bandwidth limit is still in the order of terahertz.

The serializer chip used in the demonstration has a 3.2-Gb/s throughput using ECL logic. The data rate can be improved using very simple dynamic logic if only the function of pulsewidth reduction is desired. In a simulation based on the 65-nm Berkeley Predicted Technology Model, a dynamic circuit can produce bit pulses with 50-ps duration which would be good enough for implementing beyond 15-Gb/s operation in NRZ mode. The data rate is also restricted by the throughput of the chip (SY100EP196V, Micrel) for time delay tuning. We believe that besides the transistors scaling down, the throughput of the delay chip can be enhanced by using III–V compound semiconductor, such as GaAs and InP technologies [11] or by using current mode logic [12]. Optical passive delay circuit incorporated for RZ mode operation shown in Fig. 4(c) is also a promising candidate to generate time delays with picosecond resolution [13] for any high data rate possible.

The system measured jitter is below 5 ps, which is mainly determined by the resolution of the delay chip. The FlexPhase technology from Rambus can provide 2.5-ps resolution and would be suitable for multigigahertz data transmission. Also, the delay granule would be improved as integrated circuit being further scaled down. Very low jitter can be achieved using pulse laser source for synchronization [14]

Power budget is key factor to allow high signal-to-noise ratio for a given photodetector, especially when the active area of the photodetector is shrinking with the purpose for achieving higher speed. Therefore, high-power laser source, low loss optical layer, and high efficiency collimating microoptics are preferred for implementing high-performance BIOB. If the sensitivity of 10-Gb/s photodetector is -12 dBm at 10^{-12} BER and we leave a margin of 5 dB for balancing the modulation current from different VCSEL sources, the allowed splitting loss is $3\,\text{dBm}-2.7\,\text{dB}-5\,\text{dB}-(-12\,\text{dBm}) = 7.3\,\text{dB}$, which limits the total number of daughter boards to be $10^{0.73} \approx 5$. A 2.5-Gb/s photodetector with -18-dBm sensitivity would allow almost four times (6 dB) more fan-outs, but beam divergence and substrate dimensions also impose limitations. Avalanched photodetectors [10] are desired to support more boards at 10 Gb/s. The RZ approach based on pulse laser sources could also deliver a higher power to the photodetectors because erbium-doped fiber amplifiers are available for 1550-nm pulse laser sources.

V. Conclusion

In our demonstration, we use volume photopolymer holograms as fan-in/fan-out couplers to build optical bit-interleaved backplane bus. Bit-interleaved optical bus allows multiple daughter boards to send interleaved optical bit pulses while sharing common data transmission channels, and thus, this approach can relieve the wiring congestion problem and also provide better security and reliability. The total number of daughter boards allowed in a BIOB is determined by the optical power loss and receiver sensitivity for a certain BER. Operations of a three-board BIOB in NRZ and RZ mode at data rate from 1.25 to 15 Gb/s are successfully tested.

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