Effects of Thermal-Via Structures on Thin-Film VCSELs for Fully Embedded Board-Level Optical Interconnection System

J. H. Choi, L. Wang, H. Bi, and R. T. Chen, *Fellow, IEEE*

***Abstract*—The thermal characteristics of a thin-film vertical-cavity surface-emitting laser (VCSEL) are studied both theoretically and experimentally. The thermal resistances of the VCSEL with variable thickness, ranging from 10 to 200 μm, have been determined by measuring the output wavelength shift as a function of the dissipated power. The thermal simulation results agree reasonably well with the experimentally measured data. From the thermal management viewpoint, a thinned VCSEL has an exclusive advantage due to the reduction of the thermal resistance. The thermal resistance of a 10-μm-thick VCSEL is 40% lower than that of a 200-μm-thick VCSEL. A theoretical analysis of the thermal-via effects is performed to determine the optimized thickness range of thin-film VCSEL for the fully embedded structure. The thermal resistance of the fully embedded thin-film VCSEL with closed and open thermal-via structures is also evaluated, and the suitable VCSEL thickness is reported.**

***Index Terms*—Fully embedded optical interconnection, printed circuit board (PCB), self-heat generation, thermal–electric coupled field analysis, thermal resistance, thermal via, thin-film vertical-cavity surface-emitting laser (VCSEL).**

I. INTRODUCTION

WITH the rapid evolution of the integrated circuit technology, the clock frequency and the integration density of microprocessors improve each year [1]. However, the major bottleneck of high-speed interconnections on printed circuit boards (PCBs) is the limited data transmission rate of copper transmission lines with low-K material (FR-4). At high-frequency operation (>10 GHz), the copper transmission lines on the PCB induce degradation in the rise and fall times of electrical signals, electromagnetic interference and need higher power consumption due to skin effect and impedance mismatch [2], [3]. Various ideas on optical interconnection techniques are applied to overcome the frequency-dependent loss of electrical interconnection lines [3]–[5]. Although the optical interconnections have great advantages compared to the electrical interconnections, the reliability of these systems due to packaging vulnerability is a paramount concern.

To relieve the packaging difficulty, we have developed a fully embedded board-level optical interconnection system, which is also depicted in Fig. 1 [6]–[9]. All the optoelectronic components including the vertical-cavity surface-emitting laser (VCSEL) array, p-i-n photodiode array, total internal reflection coupling mirror, and the planar polymer waveguides are integrated within the three-dimensional (3-D) interconnection layers during the conventional PCB fabrication processes. A 12-channel 850-nm GaAs VCSEL array is employed to convert the electrical signals into the optical signals. Optical signals are transmitted through a 12-channel polymer waveguide array and then converted into electrical signals by a 12-channel GaAs PIN photodiode array. Through the microvia structures, the electrical signals and the bias are transmitted from the electrical layer to the embedded optical layer and vice versa.

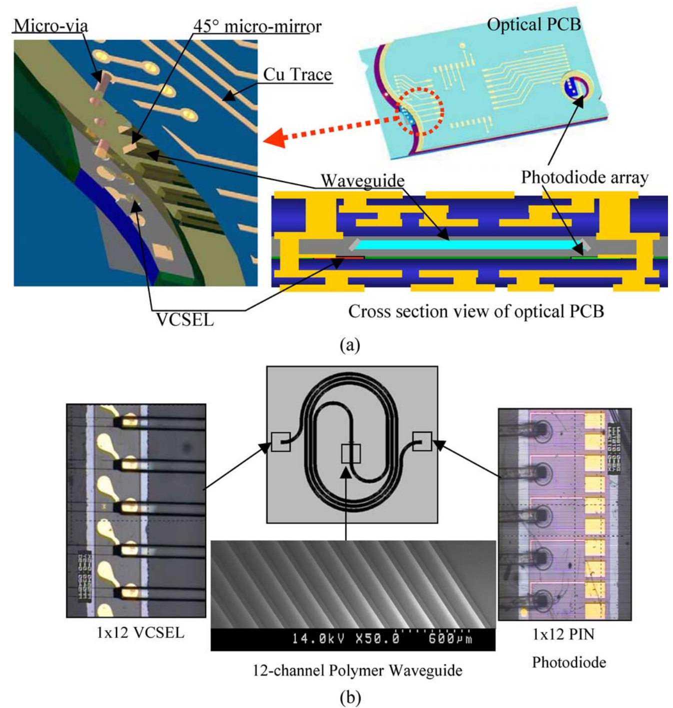

Fig. 1. Schematic diagrams of the fully embedded board-level optical interconnection system. (a) 3-D cross-sectional view of an optical layer-interposed PCB. (b) 12-channel optical waveguide film layer with an integrated thin-film VCSEL and p-i-n photodiode arrays.

In this architecture, however, the self-heating effect of the VCSEL causes critical issues in the system reliability as the integrated VCSEL arrays are surrounded by thermal insulators such as the optical polymer films (TOPAS) and PCB bonding materials (prepreg or pressure-sensitive-adhesive film). As the operating lifetime of the VCSEL decreases

Manuscript received September 2, 2005; revised May 4, 2006. This work was supported in part by the Defense Advanced Research Projects Agency, in part by the Office of Naval Research, in part by the National Science Foundation, and in part by the Texas Advanced Technology Program.

The authors are with the Microelectronics Research Center, Department of Electrical and Computer Engineering, University of Texas, Austin, TX 78712-1084 USA (e-mail: jino@mail.utexas.edu; wli@ece.utexas.edu; bihai@mail.utexas.edu; chen@ece.utexas.edu).

Digital Object Identifier 10.1109/JSTQE.2006.881903

1077-260X/$20.00 © 2006 IEEE

exponentially with temperature [10], the thermal management of the embedded VCSEL arrays is one of the prime concerns in the fully embedded optical interconnection system. Chen *et al.* [11] and Liu *et al.* [12] have reported device-level investigations on the thermal characteristics of the VCSEL. Also, comprehensive studies on the thermal resistance of an integrated VCSEL array on PCB were performed by Lee *et al.* [13], Pu *et al.* [14], and Krishnamoorthy *et al.* [15]. These papers present valuable results, but the results are not applicable to our system directly because of the different integration structures.

This paper presents the theoretical and experimental studies of the thermal characteristics of the fully embedded thin-film VCSEL array, which determines the effective thermal-via structures. The thermal resistances as a function of the substrate thickness of the VCSEL are measured experimentally. A two-dimensional (2-D) finite-element analysis is performed to simulate the temperature-field distribution near and across the active region inside the VCSEL as a function of the substrate thickness of the VCSEL and the thermal-via structure. Not only the heat generation in the active region but also the joule heating (I^2R) effect in the distributed Bragg reflectors (DBRs) are considered by the thermal–electric direct-coupled field analysis.

II. Fabrication of Thin-Film VCSEL and Measurement of Thermal Resistance $(R_{\rm th})$

A 12-channel 850-nm oxide-confined VCSEL array with 10 Gb/s each is employed as an input light source. The initial 200-μm-thick GaAs substrate of the VCSEL is removed not only for facilitating the fully embedded integration structure but also for managing the VCSEL temperature as mentioned earlier. The initial GaAs substrate of the VCSEL is reduced down to 100 μm by mechanical lapping and polishing processes. After the mechanical thinning, the thickness of the VCSEL, within the range from 100 to 10 μm, is precisely controlled by the wet chemical etching process [16]. Fig. 2(a) and (b) shows a part of the VCSEL array before and after the substrate thinning processes, respectively. The CW L–I and I–V characteristics of the 200-μm- and 20-μm-thick VCSEL are shown in Fig. 2(c). The measured threshold current and the slope efficiency are 0.7 mA and 0.55 mW/mA, respectively. The measured characteristic temperature (T_0), indicating the temperature sensitivity of the threshold current, is in the range of 150–155 K for the studied VCSEL. Fig. 3(a) shows the schematic diagram of the measurement setup for the optical properties. Fig. 3(b) shows a 10 Gb/s eye diagram of the 20-μm-thick VCSEL measured by a digital communication analyzer (HP-83480A). Electrical contact is made with micro-probes linked to a pulse pattern generator (HP-83592C). The pulse pattern generator provides the modulation by generating a $2^{23}-1$ pseudorandom bit sequence nonreturn to zero pattern at 10 Gb/s. The emitted light is collected by a multimode fiber ($\varphi = 62.5$ μm) and detected by a 21-GHz bandwidth photoreceiver (Newport, D-15). The measured 10 Gb/s eye diagram shows a reasonable opening.

Due to the self-heating effect of the VCSEL, the temperature of the active region rises relative to the heat sink. To achieve maximum VCSEL reliability in the fully embedded structure, it is imperative to control the VCSEL temperature during the operation. The ratio of the temperature rise (ΔT) to the net dissipation power $(\Delta P_{\rm diss})$ is defined as the thermal resistance $(R_{\rm th})$. The thermal resistance $(R_{\rm th})$ evaluation of the VCSEL as a function of the substrate thickness is performed by measuring the wavelength shift with both the temperature $(\Delta\lambda/\Delta T)$ and the net dissipated power $(\Delta\lambda/\Delta P_{\rm diss})$. The thermal resistance is given by

$$R_{\rm th} = \Delta T/\Delta P_{\rm diss} = (\Delta\lambda/\Delta P_{\rm diss})/(\Delta T/\Delta\lambda) \qquad (1)$$

where ΔT is the temperature rise in the active region, $\Delta P_{\rm diss}$ is the change of the electrical power dissipated in the VCSEL, and $\Delta\lambda$ is the wavelength shift. A VCSEL array is mounted on a thermoelectric cooler to precisely control the substrate temperature at $25\,^\circ\mathrm{C} \pm 1\,^\circ\mathrm{C}$. The measured wavelength–temperature variation $(\Delta\lambda/\Delta T)$ is 0.066 nm/°C. In Fig. 4, the slopes of the wavelength shift as a function of the net dissipated power $(\Delta\lambda/\Delta P_{\rm diss})$ for 200-, 100-, 60-, 20-, and 10-μm-thick VCSELs are 188, 169, 153, 144, and 120 nm/W, respectively. The experimentally measured thermal resistance values for each device are 2848, 2560, 2326, 2181, and 1830 °C/W, respectively.

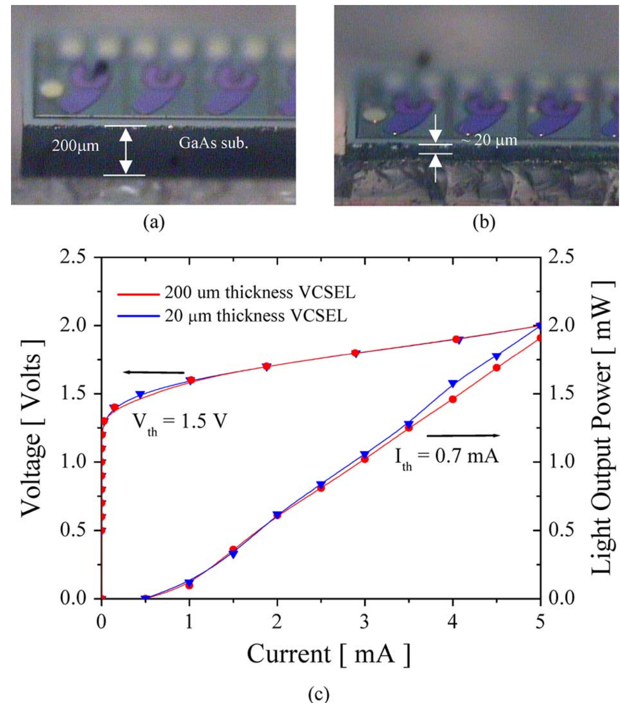

Fig. 2. (a) 200-μm-thick VCSEL array (before substrate thinning). (b) 20-μm-thick VCSEL array (after substrate thinning). (c) Electrical and optical properties of the VCSEL (eye diagram measured at 5 mA/2 V-bias condition).

III. Numerical Modeling of Self-Heating Effect for Thin-Film VCSEL

Several studies on the self-heat generation mechanisms inside the VCSEL have been reported [11], [12]. There are two major heat sources. One is the resistive joule heating when current

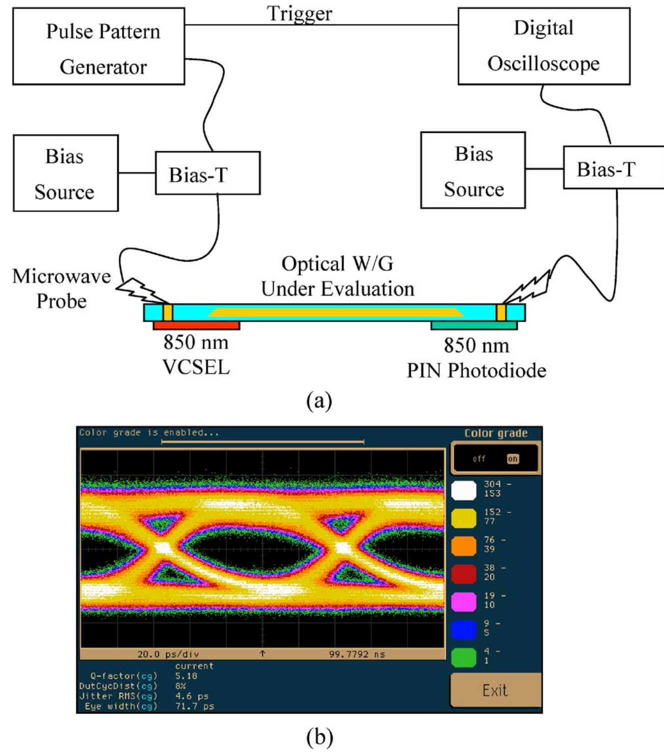

Fig. 3. (a) Schematic diagram of the speed-measurement setup. (b) 10-Gb/s eye diagram measured at 5 mA/2 V-bias condition.

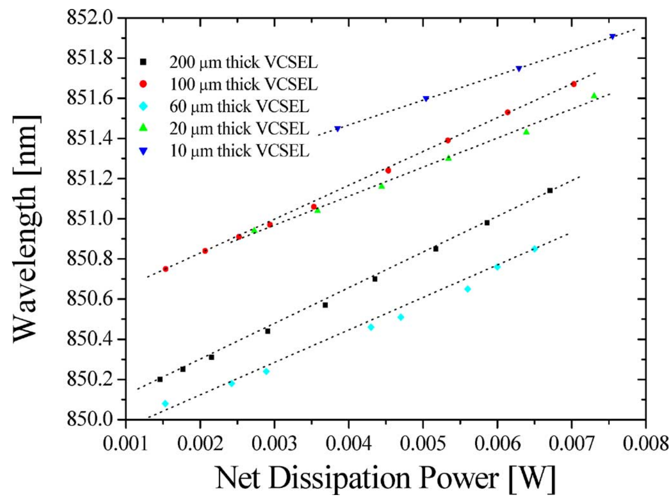

Fig. 4 Experimentally measured wavelength shift as a function of the net dissipated power.

flows through the DBRs, and the other one is the nonradiative recombination of electrons and holes in the active region. To simulate the temperature rise inside the VCSEL, the heat source distributions inside the VCSEL have to be determined. In this paper, a 2-D thermal–electric direct-coupled field analysis module in the ANSYS software is used to calculate the temperature distribution due to the joule heating in the DBRs and the nonradiative recombination in the active region. In this simulation, we assume that the VCSEL has an azimuthal symmetry. To consider the interface and boundary scattering effects of phonons

TABLE I
MATERIALS PROPERTIES AND PHYSICAL DIMENSIONS USED IN THE SIMULATION

	Thermal conductivity (W/μm-K)		Electrical conductivity (Ω^{-1}-μm^{-1})		Thick (μm)
p-DBR	k_r / k_z	1.2 X 10^{-5}/ 1.0 X 10^{-5}	σ_r / σ_z	2.016 X 10^{-3}/ 1.5 X 10^{-5}	3.30
n-DBR	k_r / k_z	1.2 X 10^{-5}/ 1.0 X 10^{-5}	σ_r / σ_z	4.03 X 10^{-2} / 2.85 X 10^{-4}	3.497
Substrate	$k_r = k_z$	4.5 X 10^{-5}	$\sigma_r = \sigma_z$	3.3 X 10^{-2}	10~200
Au	$k_r = k_z$	3.1 X 10^{-4}	$\sigma_r = \sigma_z$	45.4	0.2
Copper	$k_r = k_z$	3.86 X 10^{-4}	$\sigma_r = \sigma_z$	58.8	0~200
Polymer	$k_r = k_z$	2.0 X 10^{-7}	$\sigma_r = \sigma_z$	10^{-18}	30~100

and electrons, anisotropic material properties are used in the DBR region. Table I lists the electrical and thermal properties used in this simulation.

The thermal–electric simulation is limited to the steady-state analysis. First, the electric field analysis is performed to calculate the current density distributions inside the VCSEL near the active region. And then, the thermal analysis is conducted to calculate the joule heating and the temperature distributions inside the VCSEL. The local heat generation rate due to the joule heating is calculated by

$$q = \sigma_z \left(\frac{\partial V}{\partial Z}\right) + \sigma_r \left(\frac{\partial V}{\partial r}\right)^2 \tag{2}$$

where σ_z and σ_r are the electrical conductivities in the z axial and the radial directions, respectively [11]. A 2-V potential drop boundary condition, equivalent to our experimental work, is used for the electric field analysis. The steady-state heat conduction equation for the axial symmetric structure is governed by

$$k_z \frac{\partial^2 T}{\partial Z^2} + k_r \frac{\partial^2 T}{\partial r^2} + q(z, r) = 0 \tag{3}$$

where q is the local heat generation rate, and k_z and k_r are the thermal conductivities along the z axial and the radial directions, respectively [17].

Fig. 5(a) shows a mesh-generated 2-D modeling structure of the VCSEL near the active region. Both the Si-doped n-type DBR and the C-doped p-type DBR consist of stacks of quarter-wavelength layers of GaAs and $Al_{0.9}Ga_{0.1}As$. The current aperture and the active region are located between the two reflectors. Symmetric and adiabatic boundary conditions are applied on the sidewall and the top surface of the modeling structure. The boundary condition for the bottom surface of the Cu plate is 25 °C. The radial distributions of the temperature rise and the heat generation density near the active region are shown in Fig. 5(c). According to the electrical potential distribution inside the VCSEL, most of the voltage drop occurs across the p-type DBR. As shown in Fig. 5(b), an abrupt voltage drop near the edge of the active region indicates a strong current concentration when a great portion of the current converges into the active region. This current concentration gives rise to a heat source spike at the edge of the active region, as shown in Fig. 5(c). However, this spike-shaped heat source distribution does not cause a local temperature peak distribution. The temperature distribution peaks along the optical axis. These observations are consistent with the results of Chen [11].

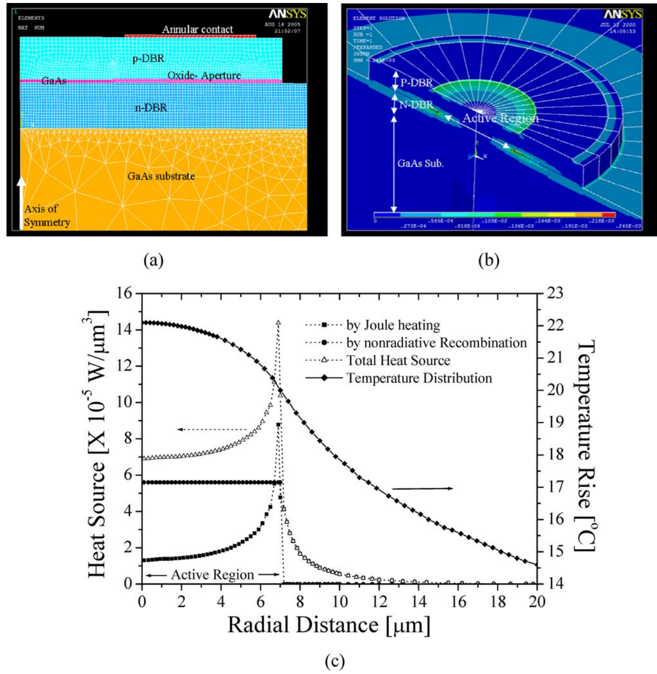

Fig. 5. (a) 2-D symmetric modeling of the VCSEL and mesh structure near the active region. (b) Current density distribution inside the VCSEL near the active region. (c) Heat source and temperature rise distributions of the 200-μm-thick VCSEL near the active region (5 mA/2 V-bias condition).

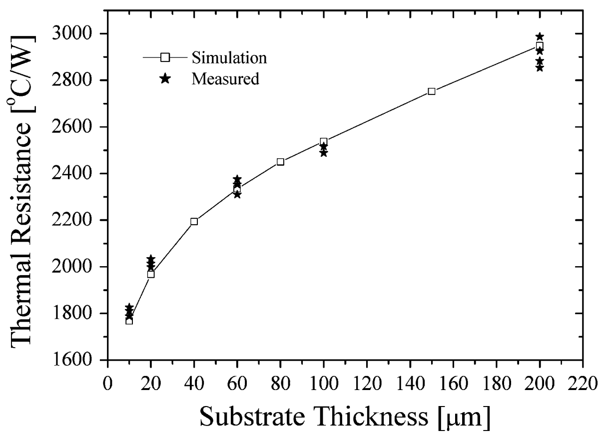

Fig. 6. Experimental and simulation results of the thermal resistances as a function of the substrate thickness of the thin-film VCSEL.

The calculated and experimentally measured thermal resistances are shown in Fig. 6 with the ambient temperature set at 25 °C. The calculated thermal resistances as a function of the substrate thickness of the VCSEL match well with the experimental results. This confirms that the simulation models for this study have been properly carried out, and the thinned VCSEL has an exclusive advantage of heat management due to the reduction of the thermal resistance. The thermal resistance of the 10-μm-thick VCSEL is 40% lower than that of the 200-μm-thick VCSEL. The calculated active region temperatures for 200-μm- and 10-μm-thick VCSELs are 47.16 °C and 38.9 °C, respectively.

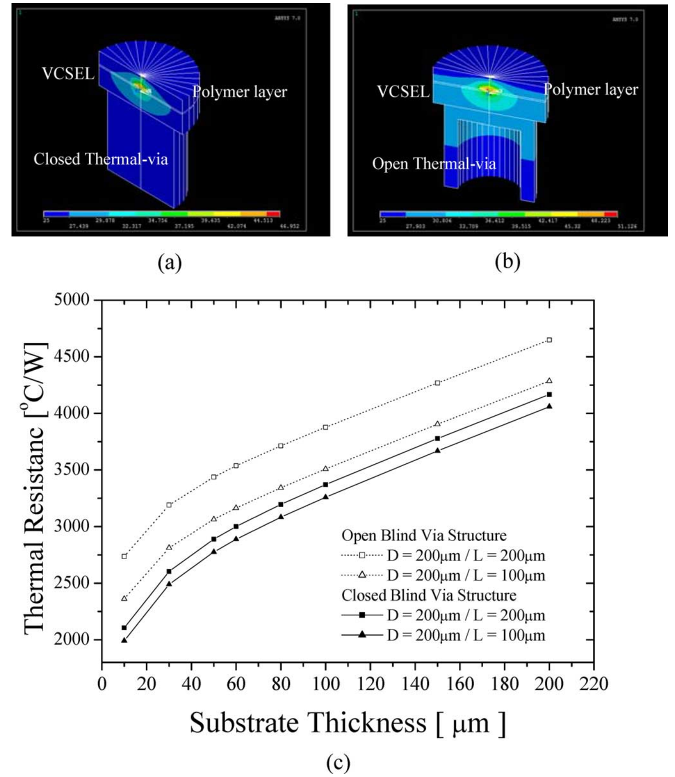

Fig. 7. (a) 50-μm-thick VCSEL with a backside closed blind-via structure. (b) 50-μm-thick VCSEL with a backside open blind-via structure. (c) Simulation results of the thermal resistance as a function of the substrate thickness of the thin-film VCSEL with different thermal-via structures.

IV. Thermal-Via Structures for the Fully Embedded Thin-Film VCSEL

Thermally, via plays a significant role in locally enhancing the heat conduction through the board as the thermal conductivity of copper is 1200 times than that of the common dielectric materials [18]. On the backside of the fully embedded thin-film VCSEL, a thermal blind via, where it enters one side and stops at an internal layer, will be applied as a heat sink structure. Fig. 7(a) and (b) shows simulation results of the temperature distribution inside the VCSEL with two commonly employed thermal-via structures, the closed blind via [copper filled inside via hole—(a)] and the open blind via [30-μm-thick copper electroplated inside via hole—(b)], respectively. In this simulation model, we assumed the top of the VCSEL to be covered by the polymer layer, which is the wave guiding layer as shown in [8] and [19].

Fig. 7(c) shows the theoretically determined thermal resistances of the fully embedded thin-film VCSEL with different thermal-via structures. Following the previous results (Fig. 6), the compatible thermal resistance for the fully embedded VCSEL structure should be in the same range as that of the 200-μm-thick VCSEL with a 25 °C substrate cooling condition. Therefore, in this study, the target thermal resistance is determined to be in the range of 2800–3000 °C/W. In the case of the open blind-via structures [straight lines in Fig. 7(c)] with an aspect ratio of 1 and 0.5, the effective substrate thickness of the thin-film VCSEL is estimated in the range of 12–22 μm

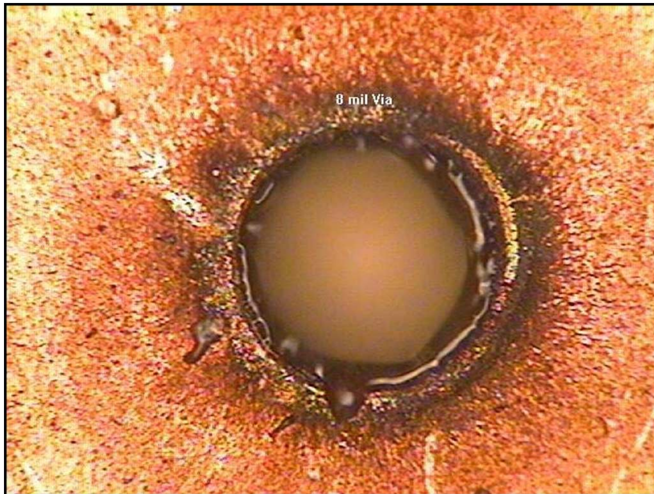

Fig. 8. Fabricated via hole on the optical film layer ($D = 200$ μm, aspect ratio = 0.5).

and 29–46 μm, respectively. Also, in the case of the closed blind-via structures [dotted lines in Fig. 7(c)] with an aspect ratio of 1 and 0.5, the fully embedded structure-compatible substrate thickness of the VCSEL is in the range of 44–60 μm and 53–72 μm, respectively. Fig. 8 shows a via-hole structure on the optical film, which was fabricated with a diameter of 200 μm and an aspect ratio of 0.5. The copper pillar inside the via hole is clearly shown. Such a thermal via will be integrated according to the scheme shown in Fig. 1. More results will be presented later.

V. Conclusion

The thermal resistances of the substrate-thinned VCSEL are experimentally measured and calculated using the 2-D thermal–electric coupled field analysis method. Both the joule heating and the nonradiative recombination effects are considered to calculate the heat source and the temperature rise distributions inside the VCSEL near the active region. The thermal–electric analysis results match well with the experimental data. The simulation models for this study are proper, and the thinned VCSEL has an exclusive advantage of heat management. The thermal resistance of the 10-μm-thick VCSEL is 40% lower than that of the 200-μm-thick VCSEL. The calculated active region temperatures for 200-μm- and 10-μm-thick VCSELs are 47.16 °C and 38.9 °C, respectively. As per the theoretical analysis of the thermal-via structures for the fully embedded thin-film VCSEL, the calculated thin-film VCSEL thickness compatible with the fully embedded board-level optical interconnection system depends on the thermal-via structures. In the case of the closed thermal-via structures, the substrate thickness of the VCSEL is in the range of 44–72 μm, which is in conformity to the fully embedded board-level optical interconnection system. This research is supported by DARPA, ONR, NSF and Texas ATP program.

References

[1] International SEMATECH, *The National Technology Roadmap for Semiconductor (ITRS)—Technology Needs*. Semicond. Ind. Assoc., San Jose, CA, 2004, International SEMATECH.
[2] N. Cravotta, "Wrestlemania: Keeping high-speed-backplane design under control," *EDN*, pp. 36–46, Aug. 2002.
[3] M. Forbes, J. Gourlay, and M. Desmulliez, "Optically interconnected electronic chips: A tutorial and review of the technology," *Electron. Commun. Eng. J.*, vol. 13, pp. 221–232, 2001.
[4] Y. Ishii, N. Tanaka, T. Sakamoto, and H. Takahara, "Fully SMT-compatible optical I/O package with microlens array interface," *J. Lightw. Technol.*, vol. 21, no. 1, pp. 275–280, Jan. 2003.
[5] P. V. Daele, P. Geerinck, G. V. Steenberge, and S. V. Put, "Optical interconnections on PCB's: A killer application for VCSEL's," in *Proc. SPIE VCSELs and Optical Interconnects*, Apr. 2003, vol. 4942, pp. 269–281.
[6] R. T. Chen, L. Lin, C. C. Choi, Y. Liu, B. Bihari, L. Wu, R. Wickman, B. Picor, M. K. Hibbs-Brenner, J. Bristow, and Y. S. Liu, "Fully embedded board-level guided-wave optoelectronic interconnects," *Proc. IEEE*, vol. 88, no. 6, pp. 780–793, Jun. 2000.
[7] C. C. Choi, L. Lin, Y. Liu, J. H. Choi, W. Li, D. Haas, J. Magera, and R. T. Chen, "Flexible optical waveguide film fabrications and optoelectronic devices integration for fully embedded board level optical interconnects," *J. Lightw. Technol.*, vol. 22, no. 6, pp. 2168–2176, Jun. 2004.
[8] J. H. Choi, W. Li, X. Wang, D. Haas, J. Magera, and R. T. Chen, "Performance evaluation of fully embedded board level optical interconnections," in *Proc. IEEE/LEOS Summer Topical Meeting Series—Optical Interconnects and VLSI Photonics*, Jun. 28–30, 2004, pp. 9–10.
[9] R. T. Chen, "Packaging enhanced board level opto-electronic interconnects," U.S. Patent 6 243 509, Jun. 2001.
[10] M. Fukuda, "Reliability and degradation of semiconductor lasers and LEDs," *J. Mod. Opt.*, vol. 39, no. 8, pp. 1799–1800, Aug. 1992.
[11] G. Chen, "A comprehensive study on the thermal characteristics of vertical-cavity surface-emitting lasers," *J. Appl. Phys.*, vol. 77, no. 9, pp. 4251–4258, May 1995.
[12] Y. Liu, W. C. Ng, K. D. Choquette, and K. Hess, "Numerical investigation of self-heating effects of oxide-confined vertical-cavity surface-emitting lasers," *IEEE J. Quantum Electron.*, vol. 41, no. 1, pp. 15–25, Jan. 2005.
[13] Y. C. Lee, S. E. Swirhun, W. S. Fu, T. A. Keyser, J. L. Jewell, and W. E. Quinn, "Thermal management of VCSEL-based optoelectronic modules," in *Proc. Electron. Compon. Technol. Conf.*, Las Vegas, NV, May. 21–24, 1995, pp. 387–392.
[14] R. Pu, C. W. Wilmsen, K. M. Geib, and K. D. Choquette, "Thermal of VCSEL's bonded to integrated circuits," *IEEE Photon. Technol. Lett.*, vol. 11, no. 12, pp. 1554–1556, Dec. 1999.
[15] A. V. Krishnamoorthy, K. W. Goosen, L. M. F. Chirovsky, R. G. Rozier, P. Chandramani, W. S. Hobson, S. P. Hui, J. Lopata, J. A. Walker, and L. A. D'Asaro, "16X16 VCSEL array flip-chip bonded to CMOS VLSI circuit," *IEEE Photon. Technol. Lett.*, vol. 12, no. 8, pp. 1073–1075, Aug. 2000.
[16] C. K. Lin, S. W. Ryu, and P. D. Dapkus, "High-performance wafer-bonded bottom-emitting 850 nm VCSEL's on undoped GaP and saphire substrates," *IEEE Photon. Technol. Lett.*, vol. 11, no. 12, pp. 1542–1544, Dec. 1999.
[17] F. P. Incropera and D. P. Dewitt, *Introduction to Heat Transfer*. New York: Wiley, 1996.
[18] A. M. Lush. (2004. May). Modelling heat conduction in printed circuit boards using finite element analysis. *Electron. Cooling* [Online]. Available: http://eletronics-cooling.com/html/articles.html
[19] L. Wang, W. Jiang, X. Wang, J. H. Choi, H. Bi, and R. T. Chen, "45° polymer-based total internal reflection coupling mirrors for fully embedded intraboard guided wave optical interconnects," *Appl. Phys. Lett.*, vol. 87, p. 141110, Sep. 2005.

J. H. Choi received the B.S. and the M.S. degrees in materials science and engineering from Hong-Ik University, Seoul, South Korea, in 1992 and 1994, respectively. He is currently working toward the Ph.D. degree in materials science and engineering at the University of Texas, Austin.

In 1994, he joined the Hyundai Central Research Institute, Suwon, South Korea. His current research interests include optoelectronic packaging and reliability of intra- and interboard-level guided-wave optical interconnection.

L. Wang received the B.E. degree in thermal engineering from the University of Science and Technology, Beijing, China, in 1992, and the M.S. degree in thermal engineering from the Institute of Engineering Thermophysics, Chinese Academy of Sciences, Beijing, in 2001. She is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering, University of Texas, Austin.

From 1992 to 1998, she was an Engineer with Beijing Central Engineering and Research Inc., working in China's iron and steel industry. Her current research interests include polymer-based micro- and nanoimprint structures for manipulation of laser beam propagation.

H. Bi received the B.S. degree from Tsinghua University, Beijing, China, in 1999, and the M.S. degree in electrical engineering from Florida State University, Tallahassee, in 2001. He is currently working toward the Ph.D. degree at the University of Texas, Austin.

From 2001 to 2002, he was a Researcher in fiber optics and waveguide diffractive photonics with Multiplex Inc., Milwaukee, WI. His research has been concerned with the development of tilted-fiber-grating-based wave monitors for wavelength-division-multiplexing applications, and grating writing automation systems. His current research interests include the high-bandwidth optical backplane, which utilizes photonic technology to perform signal transmission for supercomputers.

R. T. Chen (M'91–SM'98–F'04) received the B.S. degree in physics from National Tsing-Hua University, Hsinchu, Taiwan, R.O.C., in 1980, and the M.S. degree in physics and the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1983 and 1988, respectively.

He holds the Cullen Trust for Higher Education Endowed Professorship at the University of Texas, Austin (UT Austin). He joined UT Austin as a faculty member to start the optical interconnect research program in the Department of Electrical and Computer Engineering in 1992. Prior to his professorship at UT Austin, he was a Research Scientist, Manager, and Director of the Department of Electrooptic Engineering at Physical Optics Corporation, Torrance, CA, from 1988 to 1992. He also served as the CTO/Founder and Chairman of the Board of Radiant Research from 2000 to 2001, where he raised 18 million dollars A-Round funding to commercialize polymer-based photonic devices. He also serves as the Founder and Chairman of the Board of Omega Optics Inc. since its initiation in 2001. His research work has been awarded with 84 research grants and contracts from such sponsors as the DOD, NSF, DOE, NASA, the State of Texas, and private industry. His research topics are focused on three main subjects: 1) nano-photonic passive and active devices for optical interconnect applications; 2) polymer-based guided-wave optical interconnection and packaging; and 3) true-time-delay (TTD) wideband phased-array antenna (PAA). Experiences garnered through these programs in polymeric material processing and device integration are pivotal elements for the research work conducted by his group. His group at UT Austin has reported its research findings in more than 420 published papers including over 55 invited papers. There are 26 students who have received the Ph.D. degree in electrical engineering in his research group at UT Austin. He holds 13 issued patents. He has also served as a Consultant for various federal agencies and private companies and delivered numerous invited talks to professional societies.

Prof. Chen has chaired or been a program committee member for more than 60 domestic and international conferences organized by the IEEE, The International Society of Optical Engineering (SPIE), Optical Society of America (OSA), and PSC. He has served as an Editor or Co-Editor for 18 conference proceedings. He is a Fellow of the OSA and SPIE. He was the recipient of the 1987 UC Regent's dissertation fellowship and of the 1999 UT Engineering Foundation Faculty Award for his contributions to research, teaching, and services. During his undergraduate years at National Tsing-Hua University, he led a university debate team in 1979 which received the national championship of a national debate contest in Taiwan.