Self-Aligned Carbon Nanotube Thin-Film Transistors on Flexible Substrates With Novel Source–Drain Contact and Multilayer Metal Interconnection

Daniel T. Pham, Harish Subbaraman, Maggie Yihong Chen, *Senior Member, IEEE*, Xiaochuan Xu, and Ray T. Chen, *Fellow, IEEE*

***Abstract*—This paper presents the development and characterization of self-aligned carbon nanotube thin-film transistors (CNT-TFT) on flexible substrates. The channel consisting of dense, aligned, 99% pure semiconducting single-walled CNT is deposited using the dip-coat technique on a sacrificial substrate and then transferred on the device substrate. The source, drain, and gate structures are formed by the ink-jet printing technique. A novel source–drain contact formation using wet droplet of silver ink prior to the CNT thin-film application has been developed to enhance source–drain contact with the CNT channel. Bending test data on CNT-TFT test structures show minimal change (less than 10%) in their performance. Moreover, a special multilayer metal interconnection technology is demonstrated for flexible electronics applications. Bending test data on via test structure show change in resistance by less than 5%.**

***Index Terms*—Carbon nanotube (CNT), dip-coat technique, flexible electronics, single-walled carbon nanotube (SWCNT), thin-film transistor (TFT).**

I. Introduction

INK-JET printing technique is a simple and cost-effective method to produce electronics. It is an attractive process for flexible electronics due to its noncontact and additive deposition technique. The technique does not require sacrificial resist or liftoff layers but rather deposits materials only where needed. Soluble organic materials have been used as the channel material for several state-of-the-art flexible electronics [1], [2]. However, the carrier mobility of organic semiconductor polymers is less than 1.5 $cm^2/(V{\cdot}s)$ [3], [4]. This limits the organic polymer thin-film transistor's (TFT's) operating speed to only a few kilohertz. On the other hand, carbon nanotube (CNT)-based TFTs have seen tremendous improvements over the last five years due to their excellent mobility characteristics [5], [6]. Extremely high mobility of 100 000 $cm^2/V{\cdot}s$ of individual CNTs has been reported [6]. CNT-TFT-based devices on flexible substrates have achieved high-field mobilities using ultrapure electronics-grade CNT solutions [7], [8] by ink-jet printing technique. CNT in solution can be printed; however, it often clogs up the nozzles. Other techniques such as dielectrophoresis [9], spin coat [10], and spray [11] to form CNT-TFT have been demonstrated. These techniques yield a random network of CNTs on the substrate. However, in order to retain the attractive properties of individual CNTs, it is desirable to have densely packed, perfectly aligned, horizontal arrays of CNT thin films as the channel of the TFT device. Most of the reported aligned CNT thin films are deposited on silicon or quartz substrates via the CVD technique [12]–[14]. This deposition technique is unsuitable for flexible substrates because of the high-deposition temperature.

In this study, we fabricate CNT-TFT using a combination of ink-jet printing and stamping (for CNT layer) techniques, with self-aligned-CNT channel, novel source–drain contact, and multilayer metal interconnect.

Manuscript received June 16, 2010; revised August 12, 2010 and January 20, 2011; accepted February 28, 2011. Date of publication March 24, 2011; date of current version January 11, 2012. This work was supported in part by the NASA under Contract NNX09CA37C, in part by the Air Force Office of Scientific Research (AFOSR) under Contract FA9550-09-C-0212, and in part by the Office of Naval Research under Contract N00014-10-M-0317. The review of this paper was arranged by Associate Editor C. Zhou.

D. T. Pham is with the Microelectronics Research Center, Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX 78758 USA (e-mail: danielpham@mail.utexas.edu).

H. Subbaraman is with Omega Optics, Inc., Austin, TX 78759 USA (e-mail: harish.subbaraman@omegaoptics.com).

M. Y. Chen is with the Department of Ingram School of Engineering, Texas State University, San Marcos, TX 78666 USA (e-mail: Maggie.chen@txstate.edu).

X. Xu is with the Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX 78758 USA (e-mail: coulee.xu@gmail.com).

R. T. Chen is with the Microelectronics Research Center, Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX 78758 USA (e-mail: raychen@uts.cc.utexas.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNANO.2011.2130535

II. Fabrication Process

A. Ink-Jet Printing

Ink-jet printing is performed using the Dimatix DMP 2800 (Dimatix-Fujifilm, Inc., Santa Clara, CA) that uses piezoelectric printing cartridge (DMC-11610). The ink droplet dispensed from the ink cartridge has a nominal volume of 10 pL. One or more nozzles can be used for the printing. For small TFT structure used in this study, only one nozzle is used. For other large structures such as probing pads, via contact pads and other large elements, multiple nozzles up to 16 are used. The temperature of the platen and cartridge is set at room temperature. Silver ink from Cabot Corporation (CCI-300) is used for the source, drain, and gate electrode printing. Spin-on glass is used as dielectric ink. Customized waveform patterns in the printer are used to print silver and dielectric inks.

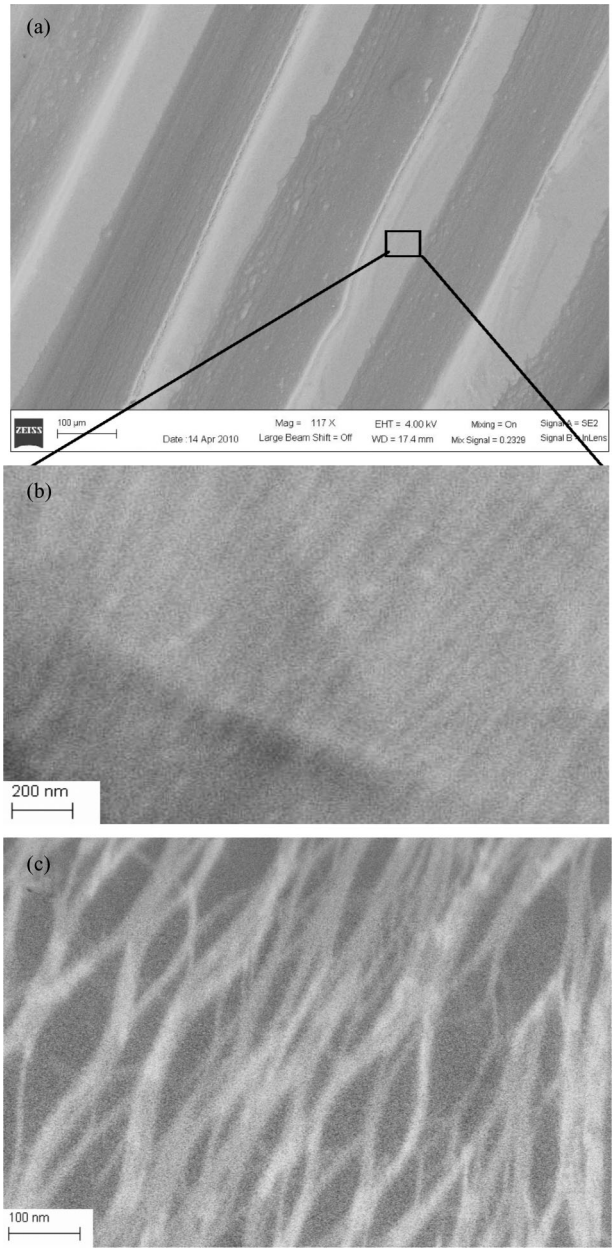
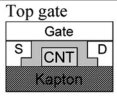
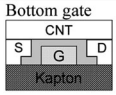


Fig. 1. (a) SEM image showing the stripe of CNT with surfactant. (b) Zoom-in SEM image of self-aligned CNT thin film with surfactant. (c) SEM image of a self-aligned CNT thin film after suspended in alcohol bath.

B. CNT Deposition

Using the dip-coat technique, CNTs can be self-aligned on the substrate [18]. The dip-coating technique has been widely used to deposit particles uniformly on different surfaces [15]–[17]. The main driving force for the convective transfer of CNTs is evaporation of the solvent. As the solvent starts to evaporate, the convection force transfers the CNTs to the contact line (solid–vapor–liquid interface), thus depositing CNTs on the substrate [15], [16]. Depending on the concentration, particle size, and drying speed, single or multiple layers can be obtained. We observe that stripes of the CNT thin film are obtained at high-drying speeds. This occurs when the capillary force, which pulls the liquid inward, builds up and exceeds the surface tension of the liquid. When this happens, a new contact line is formed as shown in Fig. 1. In this study, 99% pure semiconducting single-walled CNTsin surfactant solvent from Nanointegris, Inc., is used (S10-671, 0.1 mg in 10 mL aqueous solution) for the dip-coat technique to deposit CNTs on a silicon substrate (acting as a sacrificial substrate). The surfactants keep the CNTs from bundling with each other, which assists in the self-alignment process. Fig. 1(a) shows the SEM image of stripes of CNT, with the surfactant, formed using our process. Rinsing the substrate in 2-propanol causes the surfactants to dissolve away, thus, leaving CNT on the substrate as shown in Fig. 1(b). Further suspending the substrate in 2-propanol for 15 min entirely removes the surfactants and exposes the CNTs as shown in Fig. 1(c). Note that some amount of CNT is also lost during this process. In this process, the stripe width can be controlled by temperature (evaporation speed), solvent properties, particle density, and substrate surface roughness.

TABLE I
COMPARISON BETWEEN TOP AND BOTTOM GATE INTEGRATIONS

Integration	Advantage	Disadvantage
Top gate 	♦CNT channel deposited first ♦Dielectric & gate electrode cover the channel (passivating the channel) ♦CNT channel has good contact with the annealed source-drain metal printed on top of the channel	♦Dielectric material diffuses between CNTs and separate them ♦High thermal budget applied on the CNT channel.
Bottom gate 	♦CNT channel deposited last – No interaction with dielectric and gate materials ♦Low thermal budget for CNT channel	♦CNT channel has bad contact with source-drain areas (solution identified in this paper) ♦No passivation – exposed to air (solution identified in the paper)

C. Process Integration

Both top gate and bottom gate integration approaches are studied. Table I show the comparison of both integration schemes.

Due to its attractive advantages of low thermal budget and least interaction with dielectric and gate materials, the bottom gate integration approach is utilized in this study. In order to overcome the disadvantages, novel solutions have been addressed in this paper. The schematic of the bottom gate integration process flow is shown in Fig. 2. A Kapton polyimide substrate with a thickness of 127 μm is used. The gate electrode is first printed on the Kapton film using silver ink, followed by thermal annealing at 160 °C for 10 min. Spin-on glass is used as the dielectric material, which is also printed. The source and drain regions are printed using the same silver ink as used for gate electrode and under the same annealing conditions. The device channel length is 100 μm and width is 300 μm. For the small structure, only one nozzle is used during the printing in order to maintain resolution.

The 99% pure semiconducting CNT from Nanointegris, Inc., Skokie, IL, is deposited on the silicon substrate (as a sacrificial substrate) using the dip-coating technique, as discussed in

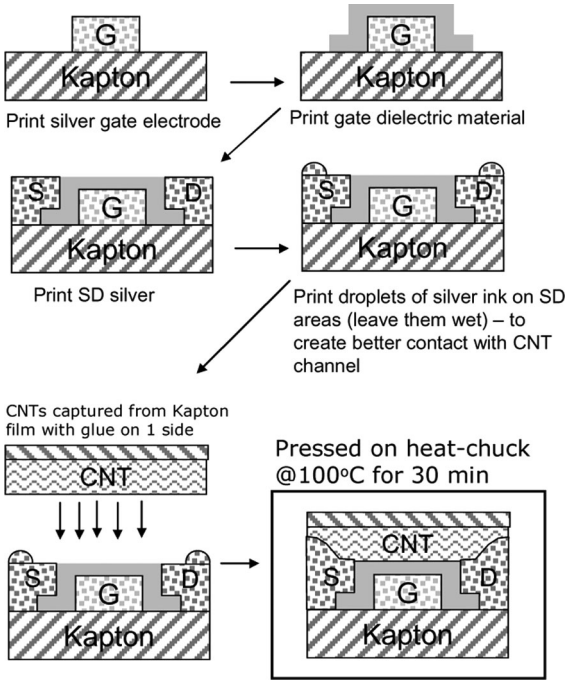


Fig. 2. Bottom gate integration with novel source–drain and CNT contact.

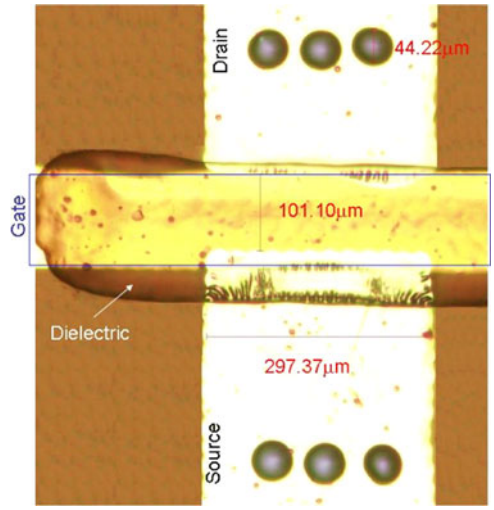


Fig. 3. Wet silver droplets on source–drain areas before bonding with a CNT thin film.

Section II-B. In order to transfer the CNT thin film onto the flexible Kapton polyimide substrate, another special Kapton substrate (25-μm thick), with adhesion coating on one side, is used to lift the self-aligned CNT thin film from the silicon substrate and lay it on top of the first substrate over the printed channel region. The Kapton with adhesive is left on the device in order to protect the CNT channel, thus, acting like a passivation layer.

Prior to bonding these two layers, a novel technique to enhance the contact between CNT and source–drain areas is developed. In this technique, droplets of silver ink are printed on the source and drain areas on the first substrate as shown in Fig. 3. These wet-silver ink droplets allow the silver liquid to "wet" the CNT thin-film area and enable good contact with the printed source and drain contact. In order to bond the two substrates, the device is left under pressure on a heat chuck surface at 100 °C for 30 min to enhance the bonding of the second Kapton substrate to the first substrate and eliminate any air pockets. Upon bonding and annealing, the source–drain contact junction is formed into the CNT thin film, thus, providing a good contact with the entire thin film. Without using the wet-silver droplets to enhance the contact, the ON current is very low ranging from a few nanoamperes to a few microamperes.

III. Characterization of the Self-Aligned CNT-TFT

Fig. 4(a) and (b) shows the measured *I–V* characteristics (I_D versus V_{DS}) of the self-aligned CNT-TFT as a function of different gate voltages V_G. The transistor *I–V* characteristics are measured using precision semiconductor parameter analyzer (Agilent 4156C). At a gate voltage of 0 V gate, the device does not show pinchoff, most likely due to a small number of metallic nanotubes in the channel. At V_G = –3 V and source–drain voltage V_{DS} of -1 V, high-drive current of 0.371 mA is obtained, which is in good agreement with the high density and self-aligned nature of CNTs on the device channel. As mentioned by Engel *et al.* [18], CNT-TFT can have the $I_{\rm on}/I_{\rm off}$ ratio as high as 10^5. At this channel length, percolation alone can give you much higher $I_{\rm on}/I_{\rm off}$ ratios; let alone using material that is highly purified. However, any improvement for the on-state current will degrade the $I_{\rm on}/I_{\rm off}$ ratio due to the increased number of metallic pathways between source and drain. In this experiment, we use a channel length of 100 μm, which is 20 times smaller than that reported in [18]. Due to the longer-channel length, a much smaller $I_{\rm on}/I_{\rm off}$ ratio can be expected from the percolation model. We experimentally observe the $I_{\rm on}/I_{\rm off}$ ratio of around 20. The restriction on the channel length comes inherently from the printing process. Further optimizations such as using the electrical burning-off technique to eliminate metallic pathways will be reported in a future publication.

Bending test is performed on the device. Fig. 5 shows the picture of bending test structures. Two different test structures are formed to evaluate the vertical and horizontal orientations of the transistor. Three different radii of curvature, 4.5, 3, and 1.5 mm, are used in this evaluation. Forward and backward bending tests are conducted as described in Fig. 5.

Fig. 6 shows the normalized drain current ($I_{D,\rm test}/I_{D,\rm original}$) plotted against the radius of curvature for the vertical test structure. In forward bending, lower drain current is observed, with up to 10% change, while no significant drain current difference is observed in the backward bending case. Larger current change for the vertical test structure can be attributed to the 300-μm channel width of the testing device subjected to the bending direction. Since the CNTs are captured by the thinner Kapton film that is bonded onto the thick Kapton substrate, forward bending may cause the thin Kapton film to move away from the substrate, while in backward bending, it causes the thin Kapton film to press against the substrate.

Fig. 7 shows drain current bending test data for the horizontal test structure. Smaller change in drain current is observed

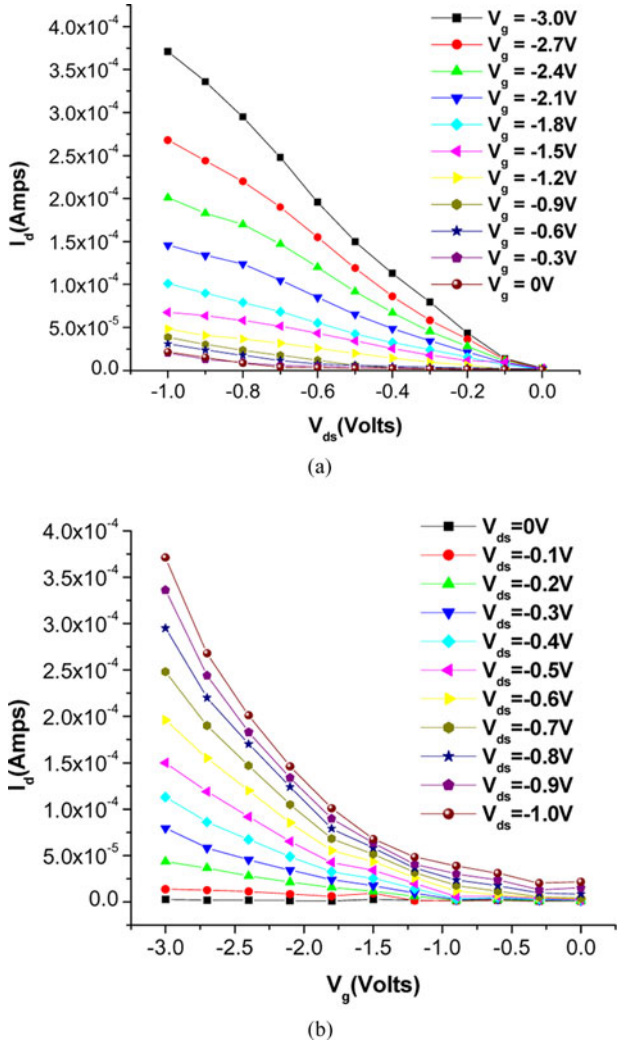


Fig. 4. (a) *I–V* characteristics (I_D versus V_{DS}) of the self-aligned CNT-TFT at different gate voltages. (b) I_D versus V_G of the self-aligned CNT-TFT.

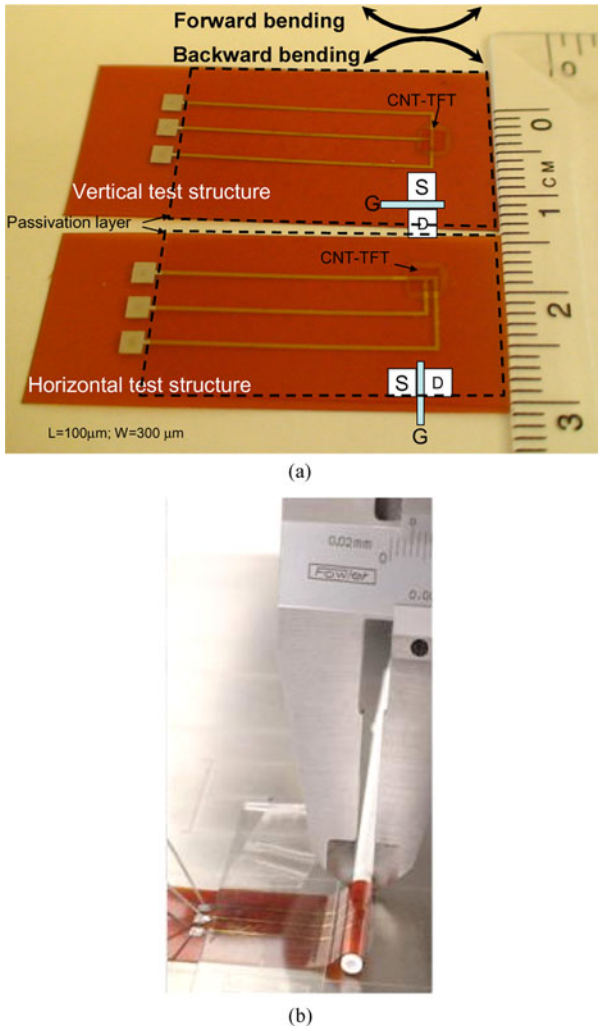


Fig. 5. (a) Bending test structure for vertical and horizontal devices. (b) Device under backward bending test at 1.5 mm radius of curvature.

(less than 6%). For the horizontal test structure, 100-μm channel length of the device is subjected to the bending direction. In the forward bending case, shorter channel length causes a small increase in current, and in the backward bending case, "stretched" channel length reduces the current (even though the thin top layer Kapton is pressed against the substrate).

IV. Multilayer Metal Interconnect

In order to develop full systems such as large area printed phased array antennas utilizing CNT-TFTs as RF amplifiers, the signal layout scheme will be extremely complicated and prohibitive if performed in 1-D (i.e., all interconnection lines, other components, and CNT-TFTs printed in the same layer). Similar to silicon semiconductor devices, such complex-flexible electronics also require multiple layers and interconnections for its circuits. Especially, CNT-TFTs will all be formed in one layer and the signals will be routed to and from these FET to all other components through various stacked layers. Therefore, considering such a requirement for futuristic applications in mind, in this paper, we also report a technique to form multiple-layer metal interconnection on flexible substrates and show multilayer interconnection to the fabricated CNT-TFT device. After forming the CNT-TFT device layer, a special Kapton substrate (25-μm thick), with adhesive coated on one side, is used to glue on top of the first substrate. Contact vias are formed prior to attaching, in order to obtain metal contacts with the gate contact pads on the bottom substrate. The via diameter used in this study is 1 mm (available cylinder blade to cut the via of that size). The adhesion of this layer is critical since any voids between layers will cause the liquid silver ink to spread between these layers due to the capillary effect. An annealing process is used after bonding these layers together by pressing against a heat chuck at 100 °C for 30 min. Then, the silver ink is printed on top of the top Kapton layer for the metal interconnection lines on the top substrate. The printed silver ink penetrates through the vias to contact the gates on the first layer. Following this, another annealing process is performed in order to evaporate the solvent in the silver ink and form a good Ohmic contact. Fig. 8 shows the schematic of multilayer metal interconnect integration for flexible electronics performed in this study.

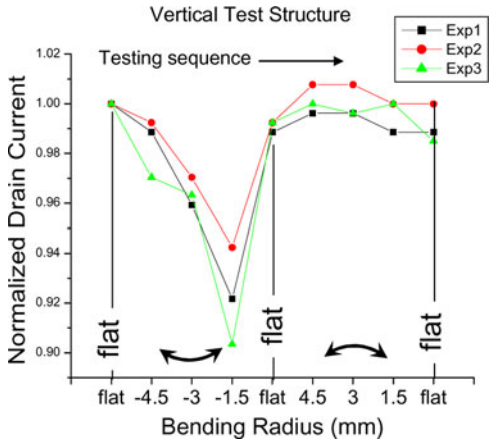


Fig. 6. Bending test data for the vertical test structure.

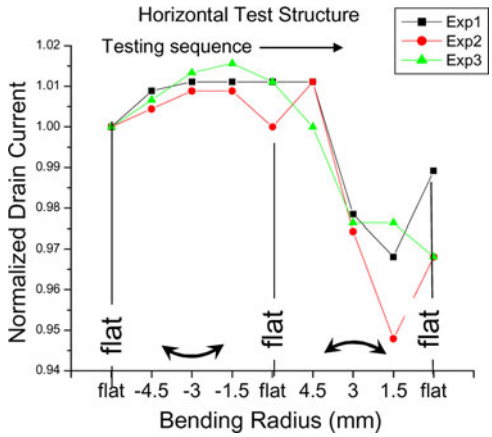


Fig. 7. Bending test data for the horizontal test structure.

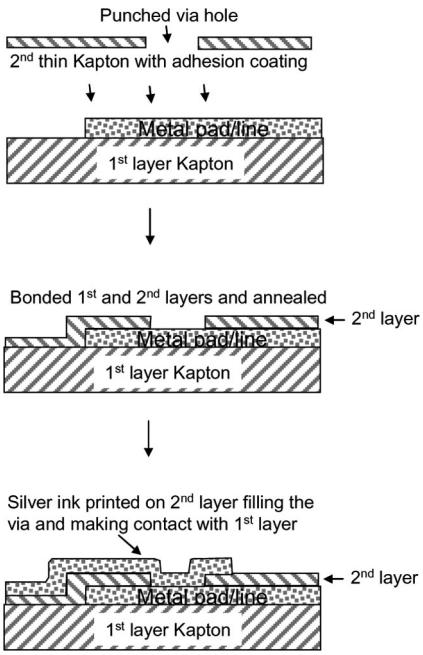


Fig. 8. Multilayer metal interconnect integration scheme.

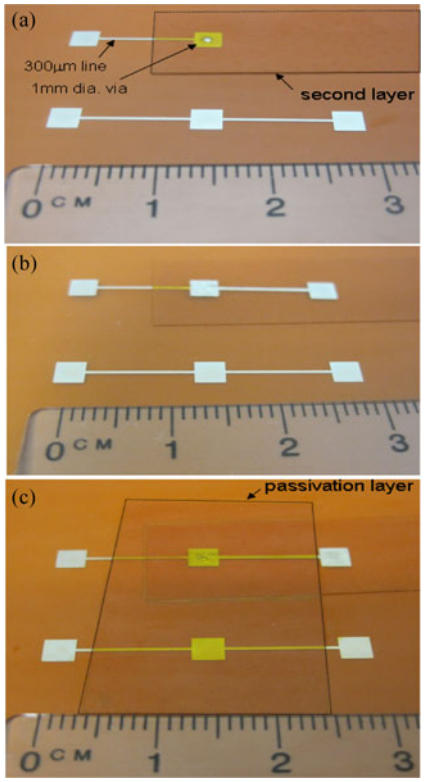


Fig. 9. (a) Via development test structure before forming via and second layer. (b) Via formed and contact line was printed on the second layer. (c) Protected or passivated layer to protect the circuit.

In order to evaluate the type of contact formed, we form a test structure as shown in Fig. 9. From the resistance measurements, we observe no resistance difference between the two contact pads with and without the interconnect via. Fig. 9(a) and (b) shows via development test structure, pre- and post silver ink printing on the second Kapton layer. To protect the metal contact line and via, the Kapton substrate with adhesive coating is bonded on top [see Fig. 9(c)]. This layer acts as a passivation or protection layer for the circuit and protects it from environment as well as mechanical strength.

Fig. 10 shows the bending test for the via test structure. Lower resistance value is observed when bending to small radius of curvature. It indicates that the via is not completely filled with silver ink. Silver thickness on flat surface is measured to be around 0.4 μm. The via diameter is 1 mm, and the metal interconnect line is 300 μm wide. In forward bending, the via might squeeze the silver particles together causing lower resistance data, while in backward bending, the top passivation Kapton layer applies pressure to the silver particles in the via.

V. Summary

In this paper, we demonstrate a self-aligned CNT-TFT using 99% pure semiconducting nanotube on flexible Kapton substrate. A novel source–drain contact is developed to enhance the contact with the CNT channel. Bending test data show minimal changes (less than 10%) in their performance.

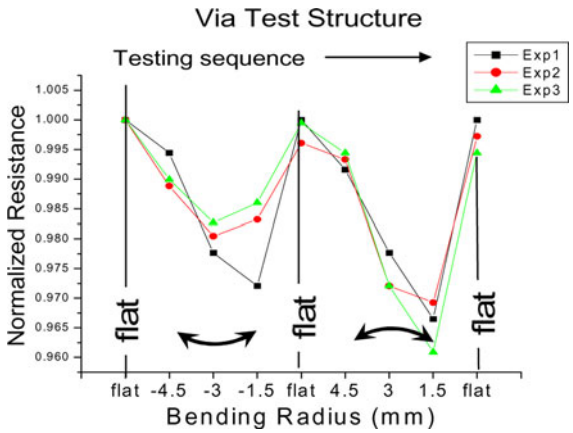


Fig. 10. Bending test data for via test structure.

Multiple-layer interconnect integration is also demonstrated on a flexible-substrate circuit. These developments lift strong constraints for flexible electronics, providing an open route for realistic applications using self-aligned CNT-TFT and multiple-layer interconnection for flexible-electronics technology.

ACKNOWLEDGMENT

The authors would like to thank Nanointegris, Inc., for their CNT solution.

REFERENCES

[1] Z. Bao, J. A. Rogers, and H. E. Katz, "Printable organic and polymeric semiconducting mat and devices," *J. Mater. Chem.*, vol. 9, pp. 1985–1904, 1999.

[2] Z. Bao and A. J. Lovinger, "Soluble regioregular polythiophene derivatives as semiconducting materials for field-effect transistors," *Chem. Mater.*, vol. 11, pp. 2607–2612, 1999.

[3] G. Wang, J. Swensen, D. Moses, and A. Heeger, "Increased mobility from regioregular poly (3-heylthiophene) field-effect transistors," *J. Appl. Phys.*, vol. 93, pp. 6137–6141, 2003.

[4] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, and W. Radlik, "High-mobility polymer gate dielectric pentacene thin-film transistors," *J. Appl. Phys.*, vol. 92, pp. 5259–5263, 2002.

[5] C. Rutherglen, D. Jain, and P. Burke, "Nanotube electronics for radiofrequency applications," *Nature Nanotechnol.*, vol. 4, pp. 811–819, Nov. 2009.

[6] T. Durkop, S. A. Getty, E. Cobas, and M. S. Fuhrer, "Extraordinary mobility in semiconducting CNT," *Nano Lett.*, vol. 4, pp. 35–39, 2004.

[7] J. Vaillancount, H. Zhang, P. Vasinajindakaw, H. Xia, X. Lu, X. Han, D. Janzen, W. Shih, C. Jones, M. Stroder, M. Y. Chen, H. Subbaraman, R. T. Ray, U. Berger, and M. Renn, "All ink-jet-printed carbon nanotube thin-film transistor on a polyimide substrate with an ultrahigh operating frequency over 5 GHz," *Appl. Phys. Lett.*, vol. 93, p. 243301, 2008.

[8] L. Nougaret, H. Happy, G. Dambrine, V. Dercycke, J.-P. Bourgoin, A. A. Green, and M. C. Hersam, "80-GHz FET produced using high purity semiconducting SWCNT," *Appl. Phys. Lett.*, vol. 94, p. 243505, 2009.

[9] S. Selvarasah, K. Anstey, S. Somu, A. Busnaina, and M. R. Dokmeci, "High flexible and biocompatible carbon nanotube thin-film trasistor," in *Proc. IEEE 9th Conf. Nanotechnol.*, 2009, pp. 29–32.

[10] M. LeMieux, M. Roberts, S. Barman, and Y. W. Jin, "Self-sorted, aligned nanotube newworks for TFT," *Science*, vol. 321, pp. 101–104, 2008.

[11] E. Artkovic, M. Kaempgen, D. S. Hecht, S. Roth, and G. GrUner, "Transparent and flexible carbon nanotube transistors," *Nano Lett.*, vol. 5, no. 4, pp. 757–760, 2005.

[12] S. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. Alam, S. Rotkin, and J. Rogers, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes," *Nature Nanotechnol.*, vol. 2, pp. 924–931, 2007.

[13] S. Kim, S. Ju, J. Back, Y. Xuan, P. Ye, M. Shim, D. Janes, and S. Mohammadi, "Fully transparent thin-film transistors based on aligned carbon nanotube arrays and indium tin oxide electrodes," *Adv. Mater.*, vol. 21, no. 5, pp. 564–568, 2009.

[14] F. Ishikawa, H. Chang, K. Ryu, P. Chen, A. Badmaev, L. Gomez, D. Arco, G. Chen, and C. Zhou, "Transparent electronics based on transfer printed aligned carbon nanotubes on rigid and flexible substrate," *ACS Nano*, vol. 3, no. 1, pp. 73–79, 2009.

[15] A. Dimitrov and K. Nagayama, "Continuous convective assembling of fine particles into two-dimensional arrays on solid surfaces," *Langmuir*, vol. 12, pp. 1303–1311, 1996.

[16] A. Dimitrov and K. Nagayama, "Steady-State unidirectional convective assembling of fine particles into two-diemnsional arrays," *Chemical Phys. Lett.*, vol. 243, pp. 462–468, 1995.

[17] M. Tao, W. Zhou, H. Yang, and L. Chen, "Surface texturing by solution deposition for omnidirectional antireflection," *Appl. Phys. Lett.*, vol. 91, p. 081118, 2007.

[18] M. Engel, J. Small, M. Steiner, M. Freitag, A. Green, M. Hersam, and P. Avouris, "Thin-film nanotube transistor based on self-assembled, aligned, semiconducting carbon nanotube arrays," *ACS Nano*, vol. 2, no. 12, pp. 2445–2452, 2008.

Daniel T. Pham received the B.S and M.S. degrees in chemical engineering from Texas A&M University and Rice University, Austin. He is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering, University of Texas, Austin.

He was engaged with the semiconductor industry for more than ten years focused in semiconductor process, device integration, and novel device research. He has more than 25 publications and eight awarded patents.

Harish Subbaraman received the B.E. degree in electronics and communication engineering from Chaitanya Bharathi Institude of Technology, Hyderabad, India, in 2004 and the M.S. and Ph.D. degrees from the University of Texas, Austin, in 2006 and 2009, respectively, both in electrical engineering.

He is currently with Omega Optics, Inc., Austin, TX. With a strong background in RF photonics and X-band phased array antennas (PAAs), he has been working on true-time-delay feed networks for PAAs and carbon nanotube-based thin-film transistors for the last four years. Throughout these years, he has laid a solid foundation in both theory and experimental skills. He was as a Principal Investigator for projects from National Aeronautics and Space Administration, Air Force Office of Scientific Research, and NAVY. He has more than 15 publications in refereed journals and conferences.

Maggie Yihong Chen (M'04–SM'08) received the Ph.D. degree of electrical engineering in optoelectronic interconnects from the University of Texas, Austin, in 2002.

She is currently an Assistant Professor of Electrical Engineering at Texas State University, San Marcos. She has more than 50 publications in refereed journals and conferences. Her research interests include optical true-time delay feeding networks for phased-array antennas, planar waveguide devices, opto-electronic interconnects, and diffractive optical elements.

Dr. Chen is a Senior Member of the SPIE.

Xiaochuan Xu He received the B.S. and M.S. degrees in electrical engineering from Harbin Institute of Technology, Harbin, Heilongjiang, China. He is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering, University of Texas, Austin.

Ray T. Chen (M'91–SM'98–F'04) received the B.S. degree in physics from National Tsing-Hua University, Hsinchu, Taiwan, in 1980 and the M.S. degree in physics and the Ph.D. degree in electrical engineering in 1983 and 1988, respectively, both from the University of California, Oakland.

He holds the Cullen Trust for Higher Education Endowed Professorship at University of Texas (UT), Austin, and the Director of Nanophotonics and Optical Interconnects Research Laboratory, Microelectronics Research Center. He is also the Director of a newly formed Air Force Office of Scientific Research Multidisciplinary Research Initiative (MURI) Center for Silicon Nanomembrane involving faculty from Stanford, University of Illinois at Urbana-Champaign, Rutgers, and UT Austin. He joined UT Austin as a Faculty Member to start optical interconnect research program in the Department of Electrical And Computer Engineering in 1992. Prior to the UT's Professorship, he was a Research Scientist, Manager, and Director of the Department of Electro Optic Engineering, Physical Optics Corporation, Torrance, CA from 1988 to 1992. He was also the Chief Technical Officer/Founder and Chairman of the Board of Radiant Research from 2000 to 2001 where he raised 18 million dollars A-Round funding to commercialize polymer-based photonic devices involving over 20 patents, which was acquired by Finisar in silicon valley (NASDAQ: FNSR). He was also the Founder and Chairman of the Board of Omega Optics, Inc., since its initiation in 2001. Over five million dollars of research funds were raised for Omega Optics.. The research topics are focused on three main subjects:nanophotonic passive and active devices for optical phased array and interconnect applications; thin-film guided-wave optical interconnection and packaging for 2-D and 3-D laser beam routing and steering; and true time delay wide-band phased array antenna. Experiences garnered through these programs in polymeric material processing and device integration are pivotal elements for the research work conducted by his group. His group at UT Austin has reported its research findings in more than 540 published papers including over 60 invited papers. He holds 20 issued patents. He has chaired or been a program-committee member for more than 100 domestic and international conferences organized by the IEEE, the International Society of Optical Engineering (SPIE), Optical Society of America (OSA), and Photonics Society of. Chinese-Americans (PSC). He was as an editor or coeditor for 18 conference proceedings. He was also as a consultant for various federal agencies and private companies and delivered numerous invited talks to professional societies.

Dr. Chen is a Fellow of the OSA and the SPIE. He was the recipient 1987 UC Regent's Dissertation Fellowship and of 1999 UT Engineering Foundation Faculty Award for his contributions in research, teaching, and services. He is also the recipient of 2008 IEEE Teaching Award. Back to his undergraduate years in National Tsing-Hua University, he led a university debate team in 1979, which received the National Championship of National Debate Contest in Taiwan. There are 33 students received the EE Ph.D. degree in his research group at UT Austin. His research work has been awarded with 99 research grants and contracts from such sponsors as Department of Defense (DOD), National Science Foundation (NSF), DOE, National Aeronautics and Space Administration (NASA), the State of Texas, and private industry.