2D silicon-based surface-normal vertical cavity photonic crystal waveguide array for high-density optical interconnects

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ABSTRACT

In this paper, we present the design guidelines, fabrication challenges and device evaluation results of a surface-normal photonic crystal waveguide array for high-density optical interconnects. We utilize the slow light effect of photonic crystals to increase the effective interaction length between photons and medium, which in turn can be used to decrease the physical length and make compact devices. The effect of the structural parameters variations on the guided mode are studied in order to provide a guideline for fabrication. Photonic crystal waveguides are vertically implemented in a silicon-on insulator substrate. Our structure possesses advantages such as universal design, CMOS compatibility, and simple fabrication process, suitable for high dense on-chip applications. Transmission results show increase of power near 1.67 μm wavelength, which agrees with our simulation results.

Keywords: Photonic crystal waveguides, nanophotonics, effective interaction length

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1. INTRODUCTION

Since the 1980s, copper-based electrical interconnects have been predicted as a bottleneck for microprocessor and computer system performance [1]. This bottleneck is mainly due to the increase in capacitance and resistance as they scale down, resulting in increased latency, power consumption as well as decreased bandwidth [2]. To address these issues, optical interconnects have been considered a strong candidate to meet the requirements for both on and off-chip applications [3-5]. Area budget, power consumption and CMOS compatibility are some of the key requirements for successful intrachip optical interconnect [6]. Conventional planar waveguides face limitations in density as well as complex fabrication process when attempting to design a $N \times N$ array structure. In this paper, we present a compact array of surface-normal photonic crystal waveguides (PCWs) utilizing slow light which can be fabricated in one CMOS compatible lithographic step.

2. DESIGN

The operating mechanism behind the surface-normal PCW is similar to a hollow-core photonic bandgap fiber (HCPBF), where a photonic bandgap (PBG) is created due to the presence of periodic air holes in a high index cladding material surrounding the center core [7]. Targeted wavelength range of light is guided through this air core by photonic band gap (PBG) guidance [8]. It is different from conventional waveguides where light travels in a high refractive index core through total internal reflection (TIR). Schematic of the surface-normal PCW array is shown in Fig 1(a). Unlike HCPBF, where the index contrast (Δn) between air and silica is less than 1, surface-normal PCWs in a suitable high-index material such as silicon, provides a high index contrast of 2.45, thus creating wider bandgaps. To incorporate the slow light effect of PCWs, we investigated the core-guided and surface modes of our structure using RSoft simulation software, which is shown in Fig. 1(b) [9]. We observe a nearly flat slope at the edge of the bandgap, which corresponds to very large group index (1/slope = n_g). Studies have shown that surface-normal PCW structure can achieve group

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indices [10]. Large group index of our structure increases the effective photon-medium interaction length (L_e), which is given by $L_e = L \times n_g$. This in turn allows for shorter physical waveguide length (L) which can further reduce the loss, leading to low power consumption.

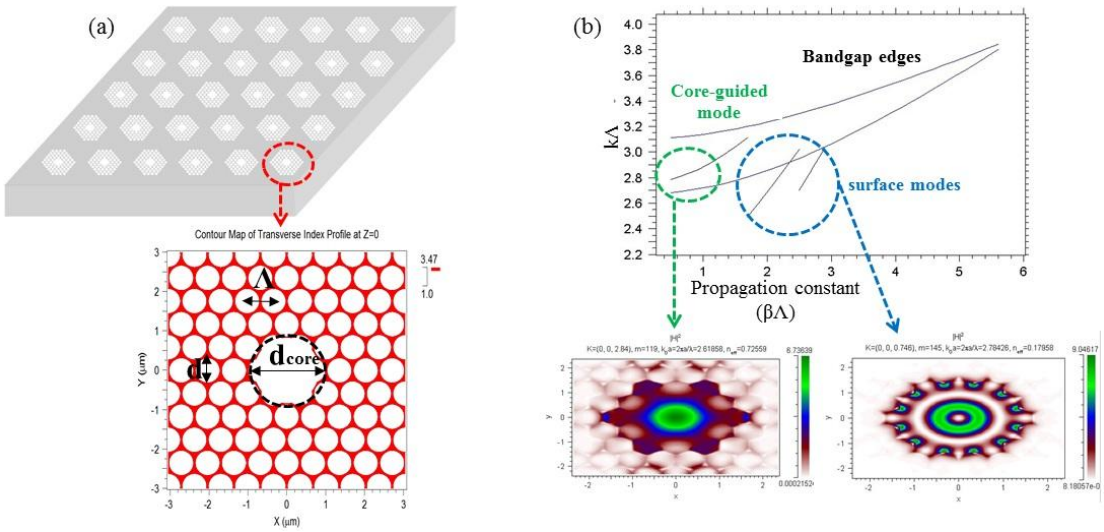

Figure 1 (a) Schematic of surface-normal PCW array (b) 2-D bandgap and different mode plots of surface-normal PCW.

One advantage of the surface-normal PCW array is its simple fabrication procedure, shown in Fig. 2. Unlike planar waveguide structures, a $N \times N$ surface-normal PCW array only requires one lithographic process, thus greatly simplifying the fabrication steps as illustrated in Fig 2(b). Another highlight of surface-normal PCWs is that the group index can be easily changed by filling the air holes with other materials or by modulating the index of silicon via thermo-optic (TO) tuning (TO coefficient of silicon = $2.4 \times 10^{-4} / K$) [10]. Also, different CMOS compatible semiconductors such as germanium or Ⅲ-Ⅴ materials can be utilized depending on applications. To fabricate an array of nearly vertical PCW structure, we utilize a two-step Bosch process involving an alternating repetitive steps of polymer passivation to protect the sidewalls, and plasma ionic etch of silicon using SF_6. Etch profiles

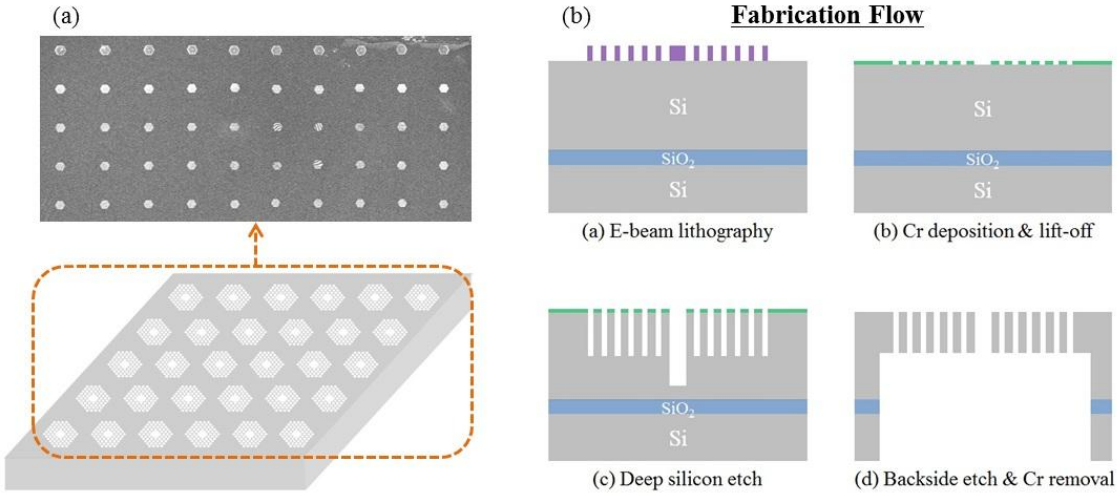

Figure 2 (a) (Top) Scanning electron microscopy (SEM) image of an actual fabricated surface-normal PCW array (bottom) schematic of PCW array (b) Schematic of fabrication process.

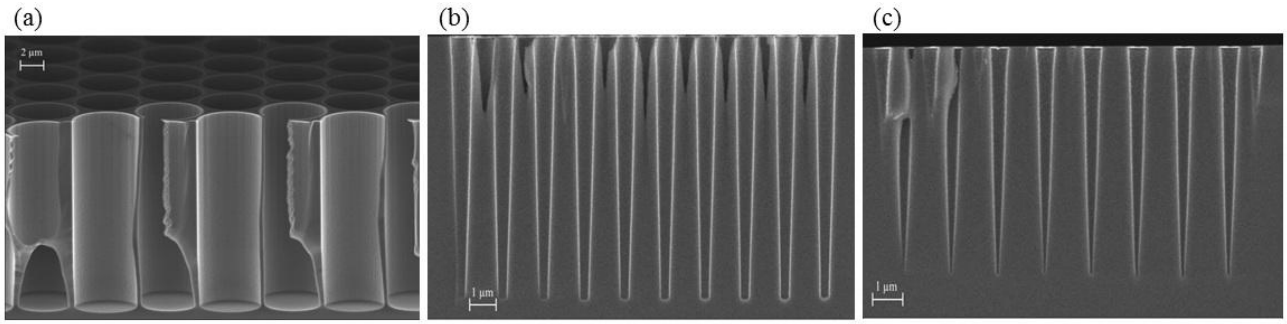

Figure 3. Cross sectional SEM image of two-step Bosch process. Hole diameters are (a) 4 µm, (b) 0.8 µm, and (c) 0.55 µm.

for different hole diameters using the Bosch process are shown in Fig 3. The tapering effect is noticeable as hole diameters decrease. This is caused by reduced number of ions penetrating through the smaller openings, and this phenomenon is also known as Aspect-Ratio Dependent Etch (ARDE) [11]. Because of the tapering effect, photons traveling through the air waveguide will experience a shift in the bandgap, which is depicted in Fig 4. For an operation wavelength of 1.67 µm, the PC diameter tolerance is about 30 nm. This, in turn, provides a guideline for fabrication and the tapering effect which can be tolerable.

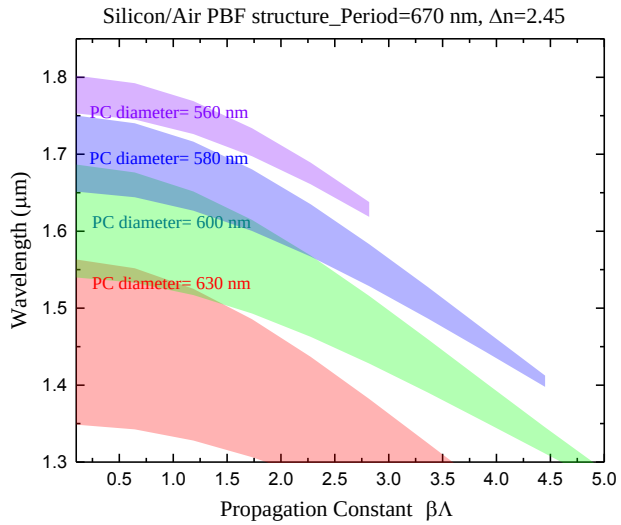

Figure 4. 2-D bandgap plot for different photonic crystal diameters. Period(Λ) is kept constant at 670 nm.

We have also checked the relationship between center core diameter (d_{core}) and guided modes to ensure slow light effect within the bandgap, which is shown in Fig 5. As d_{core} increases, the guided mode shifts away from the bandgap and eventually becomes leaky modes, which will eliminate the slow light effect. Also, the number of the surface modes is proportional to d_{core} ,in which case, the increase in the number of surface modes will make coupling more difficult.

3. DEVICE FABRICATION

As shown in in Fig. 2(b), surface-normal PCW array is fabricated using an SOI wafer which consists of 20 µm of top silicon and 1 µm of silicon dioxide layer. After Piranha cleaning, surface-normal waveguides are patterned using lectron-beam lithography follow by chrome mask deposition and lift off. Chrome mask is used because of its inertness during

the Bosch process and clean, easy removal. Various parameters (voltage, pressure, time etc.) determining the etch condition have been optimized to achieve nearly vertical profile [12]. Fig 6 (a) & (b) show the top and cross-sectional SEM images of the surface-normal PCW after etching. Due to ARDE, we see that the center hole etches deeper with

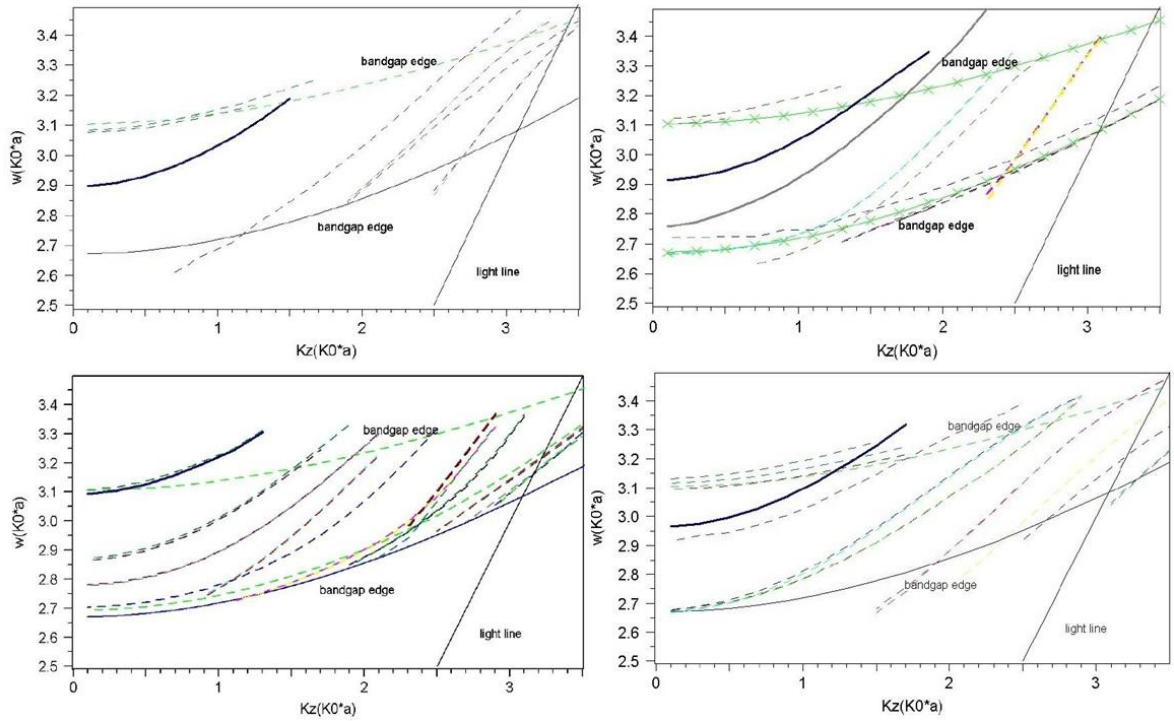

Figure 5. Full 2-D bandgap plot including core-guided mode(solid line) and surface modes(dotted lines) for various center defect hole diameters. From upper left to clockwise, the diameters are 1.25, 1.54, 1.75 and 2.02 μm, respectively.

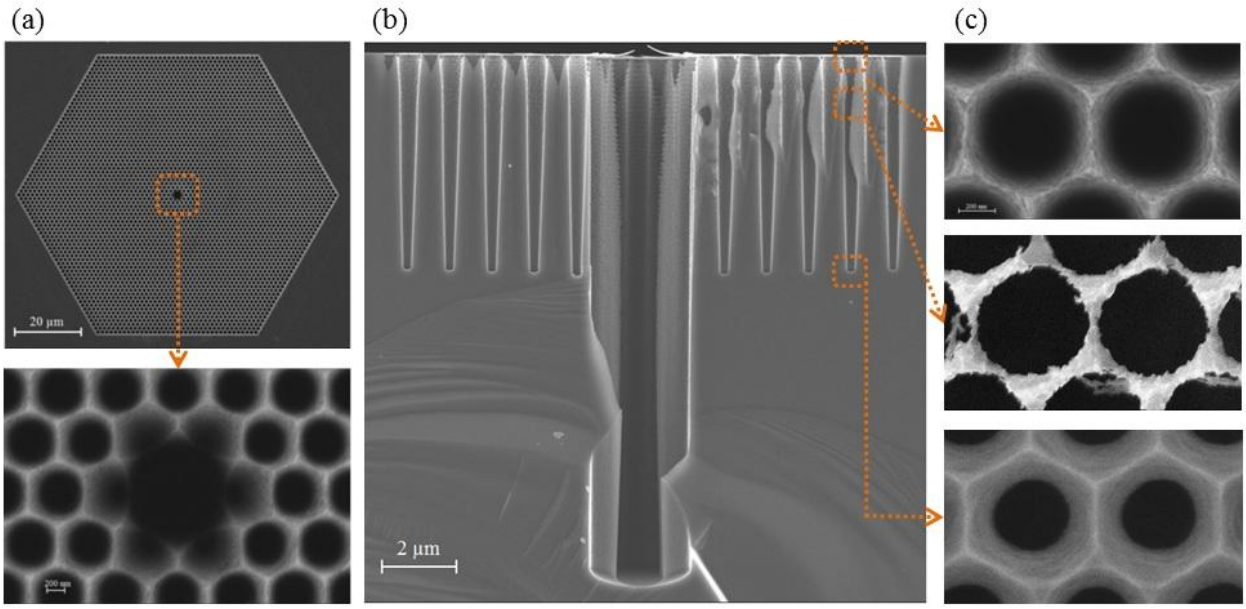

Figure 6 (a) SEM image of surface-normal PCW after fabrication (b) Cross-sectional SEM image of surface-normal PCW before etch-back technique (c) SEM images of photonic crystal along the trench

little tapering effect compared to the photonic crystal region as shown in Fig 6(b). To alleviate this mismatch in depth and to meet the diameter tolerance previously studied, we have conducted further backside etching by an etch-back technique. Fig 6(c) shows the SEM images at three different locations along the periodic trench. The tolerance between the first and second SEM image is 30 nm, which meets the requirement for maintaining the bandgap across the vertical channel at λ=1.67 μm.

4. DEVICE CHARACTERIZATION

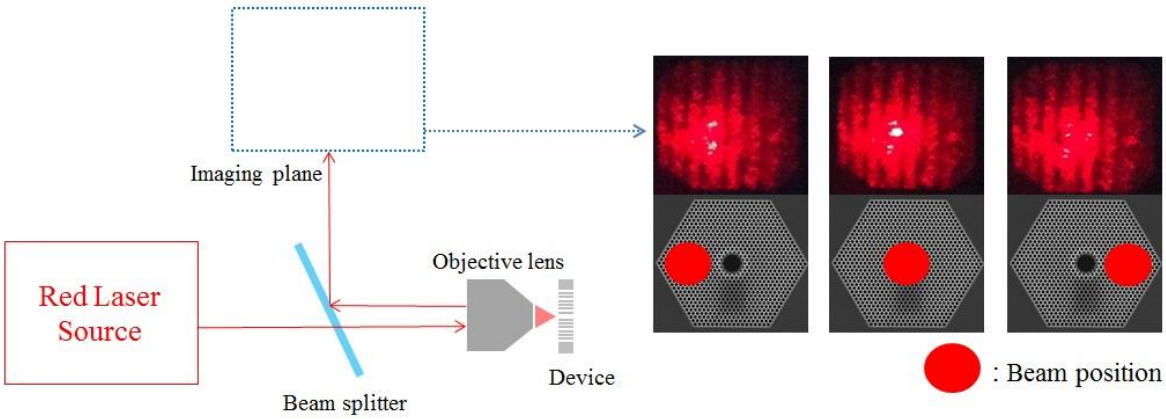

Figure 7 (a) Schematic setup for device alignment. (b) Optical image shown on imaging plane and its corresponding beam position marked on top of the SEM image of actual device.

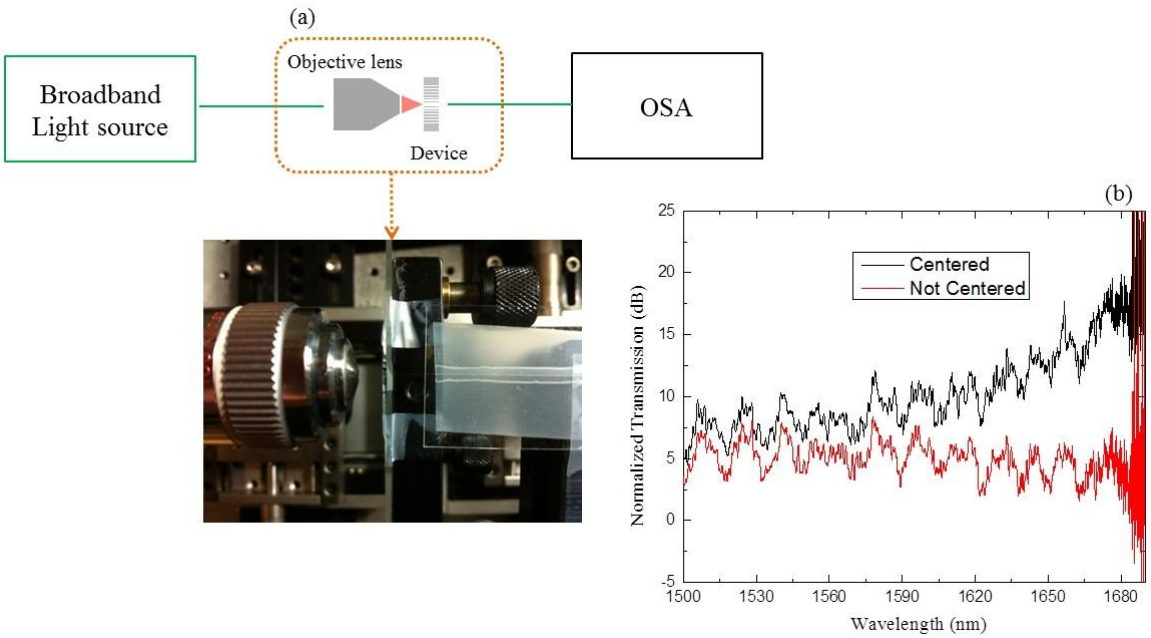

Figure 8 (a) Schematic setup for transmission measurement. (b) Normalized transmission data for aligned & misaligned case

Fig 7(a) illustrates the measurement setup for device characterization. The first procedure is to align the objective lens (100×) with the output fiber. After alignment, we move the output fiber away from the objective lens and insert the device in between. Alignment of the center core with respect to the input beam is conducted by using a red laser source with a beam splitter. The PCW face structure is observed on an imaging plane. At the location where imaging plane shows a bright spot as shown in Fig 7(b), the output power is at maximum value, further validating that the beam is aligned to the center core. To evaluate our device, input light from a broadband light source (λ=600~1750 nm) and observe the transmission at different locations of the surface-normal PCW. Fig 8(a) illustrates the schematic for transmission measurement and the transmission result is represented at Fig 8(b). The transmission spectrum shows an increase in power at the center hole compared to when the beam is not centered, for wavelengths range between 1650~1680 nm. This region also corresponds to our designed bandgap range, thus indicating that light is being guided through the surface-normal PC via bandgap effect. Further investigation of the slow light effect is under way and will be reported in a future publication.

5. CONCLUSION

In conclusion, we have successfully fabricated and tested the surface-normal PCW array on SOI wafer, which can potentially be applicable for high-density optical interconnects. By utilizing slow light effect, we are able to achieve long photon-medium interaction length within a short waveguide length, thus allowing us to increase the density and compactness on a single layer. Investigation of PC diameter size dependence of bandgap as well as the relationship between the core diameter and guided mode was conducted and provided a guideline for fabrication. CMOS compatible $N \times N$ array of PCWs can be created by only one lithographic step, thus greatly reducing the fabrication complexity. Evaluation of individual surface-normal PCW was done by aligning the beam and measuring the transmission spectrum. Preliminary measurement show an increased power from the core was observed for wavelength falling within photonic bandgap.

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