Inter-layer grating coupler on double-layer silicon nanomembranes

Yang Zhang[1,] *, David Kwong[1], Xiaochuan Xu[1], Amir Hosseini[2], Sang Y. Yang[3], John A. Rogers[3], and Ray T. Chen[1]

[1]Microelectronic Research Center, Department of Electrical and Computer Engineering, the University of Texas at Austin, Austin, USA

[2]Omega Optics, Austin, USA

[3]Department of Material Science and Engineering, Beckman Institute, and Frederick Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Urbana, USA

*yangzhang@utexas.edu

***Abstract*—We present an adhesive bonding process to fabricate on-chip, double-layer, single crystalline silicon nanomembranes. Inter-layer coupling efficiency of 25% with 35 nm 3dB bandwidth is demonstrated using subwavelength nanostructure based grating couplers.**

Keywords-Inter-layer grating coupler; silicon nanomembrane; subwavelength nanostructure

I. Introduction

Vertical integration of multiple layers of photonic components can resolve the problem of limited bandwidth density on a single-layer silicon photonic integrated circuit (PIC). Double-layer silicon PICs were previously achieved by depositing hydrogenated amorphous silicon or poly crystalline silicon [1, 2]. On-chip inter-layer grating coupling was accomplished with amorphous silicon layers [3], but single crystalline silicon layers are preferable because of their lower material absorption loss and higher carrier mobility. Adhesive bonding, which has been used in fabricating grating couplers on silicon nanomembranes [4], serves as a good candidate for fabricating double-layer silicon PICs.

In this paper, we demonstrate a method to fabricate on-chip, double-layer, single crystalline silicon nanomembranes using adhesive bonding. Inter-layer coupling between silicon nanomembranes are demonstrated using grating couplers. The grating couplers are based on subwavelength nanostructures (SWNs), whose refractive index can be engineered to accommodate grating coupler designs [5].

II. Device Design

Fig. 1 shows a 3D schematic of our inter-layer grating coupler. Input light is coupled from a waveguide on bottom layer to a waveguide on top layer through the inter-layer grating coupler. The gratings on both layers are formed by periodically replacing parts of silicon layer with SWNs, as shown in the enlarged part in Fig. 1. SWNs' refractive indices can be tuned by varying the width of the rectangular etched hole (W_{sub}) while keeping the period of SWN (Λ_{sub}) the same [6]. The SWNs were treated as a material with variable refractive index in the inter-layer grating coupler design described below.

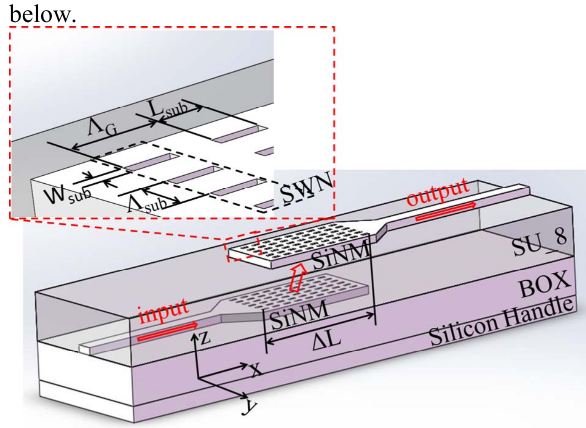

Figure 1. Schematics of the inter-layer grating coupler and the SWN.

We used 25 periods and 50% grating duty cycle for gratings on both layers. Grating period (Λ_G), bottom layer SWN's refractive index (n_{sub1}), top layer SWN's refractive index (n_{sub2}), SU-8 layer thickness (t_{SU-8}) and effective length (ΔL), which is defined as the distance between the start of the grating on the bottom layer and the end of the grating on the top layer, were optimized by 2D finite-difference-time-domain (FDTD) simulations. The input light at the bottom layer is assumed to be transverse-electric (TE) polarized. We found that the maximum coupling efficiency of the inter-layer grating coupler is 21% at 1557 nm wavelength with Λ_G=820 nm for the gratings on both layers, n_{sub1}=2.5, n_{sub2}=2.55, t_{SU-8}=3.7 μm and ΔL= 11.9 μm. In order to get the target n_{sub}, we used 26 periods and Λ_{sub}= 390 nm for the SWNs on the bottom layer,

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and 32 periods and Λ_{sub}= 390 nm for the SWNs on the top layer. W_{sub} on the bottom layer and the top layer were calculated to be 141 nm and 70 nm, respectively, with the method described in [5].

III. DEVICE FABRICATION

The device fabrication process is illustrated in Fig. 2. The gratings on the bottom layer were fabricated on a silicon-on-insulator (SOI) chip with 250 nm device layer and 3μm buried oxide (BOX) using electron beam lithography (EBL) and reactive ion etching (RIE). Another bare SOI chip, served as donor substrate, was bonded to the recipient substrate fabricated before using SU-8 based adhesive bonding. The SU-8 layer thickness can be controlled by spin-on speed. After that, the silicon handle of the donor substrate was removed by mechanical polishing and deep RIE, followed by removal of the BOX layer using wet etching. Finally, the gratings on the top layer were fabricated using EBL and RIE.

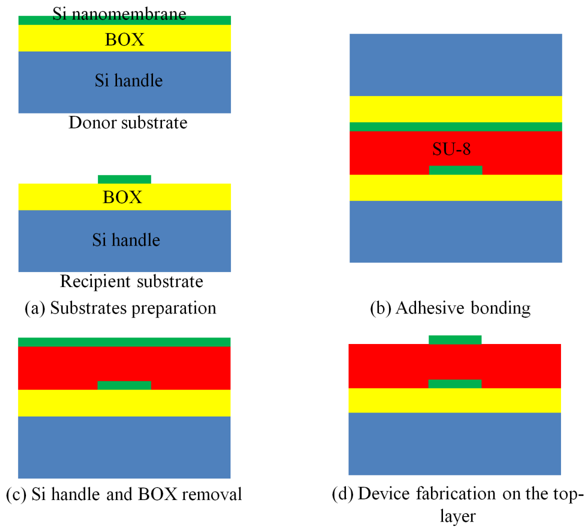

Figure 2. A schematic of the fabrication process flow.

IV. DEVICE CHARACTERIZATION

The testing setup is shown in Fig. 3. TE polarized, broad band amplified spontaneous emission (ASE) signal is coupled into the PIC, which consists of four gratings, through the input grating coupler, and finally coupled out through the output grating coupler to an optical spectrum analyzer. The collected signal was normalized to the input signal to get the total efficiency of four gratings combined. By subtracting the coupling efficiencies of the input and output grating couplers, which were measured to be 17% and 44%, respectively, through separate measurements, from the total efficiency, we obtained the coupling efficiency of the inter-layer grating coupler. Note that the tilting angles of the input and output fibers were adjusted to be 10° and 14° from the normal incidence, respectively, so that the peak efficiencies of the input and output grating couplers appear around target wavelength of 1557 nm.

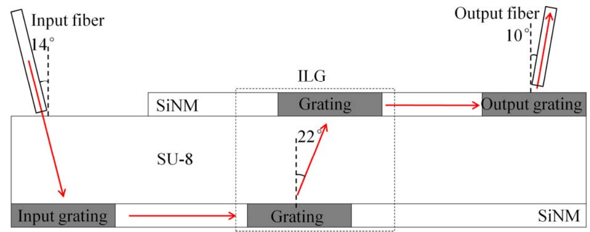

Figure 3. A schematic of the testing setup.

The measured inter-layer grating coupler has an efficiency of 25% (-6.0 dB) at 1560 nm wavelength, and a 3dB bandwidth of 35 nm, as shown in Fig. 4. In summary, we have demonstrated on-chip, inter-layer coupling with an efficiency of 25% using SWN based grating couplers between single crystalline silicon layers.

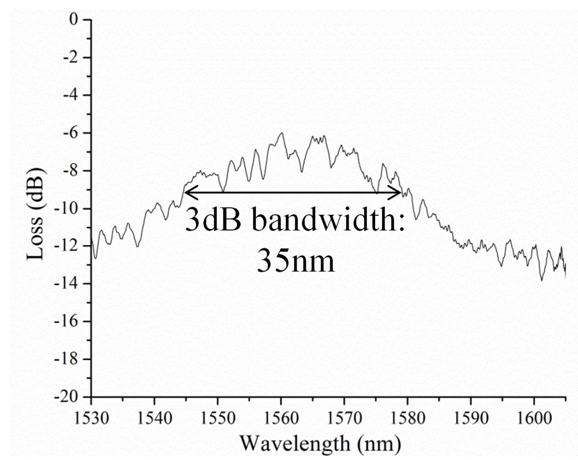

Figure 4. Measure coupling efficiency of the inter-layer grating.

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