

Vertically Integrated Double-layer on-chip crystalline silicon nanomembranes based on adhesive bonding

Yang Zhang^{1a}, David Kwong^a, Xiaochuan Xu^a, Amir Hosseini^b, Sang Y. Yang^c,
John A. Rogers^c, Ray T. Chen^{1a}

^aMicroelectronic Research Center, Department of Electrical and Computer Engineering, The University of Texas, 10100 Burnet Rd., Austin, TX 78758, USA; ^bOmega Optics, Inc, 10306 Sausalito Dr., Austin, TX 78759, USA; ^cDepartment of Materials Science and Engineering, Beckman Institute, and Frederick Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Illinois 61801, USA

ABSTRACT

In this paper we demonstrate a three-dimensional (3D) photonic integration scheme based on crystalline silicon. We develop a process using SU-8 based adhesive bonding to fabricate vertically stacked, double-layer silicon nanomembranes. A single-layer silicon photonic integrated circuit fabricated on a silicon-on-insulator (SOI) chip and a bare SOI chip are bonded together, followed by removal of the bare SOI chip's silicon substrate and buried oxide layer, to form a silicon nanomembrane as a platform for additional photonic layer. We designed and fabricated subwavelength nanostructure based fiber-to-chip grating coupler on the bonded silicon nanomembrane, and also inter-layer grating coupler for coupling between two silicon nanomembranes. The fiber-to-chip grating coupler has a peak efficiency of -3.9 dB at 1545 nm operating wavelength with transverse-electric (TE) polarization. The inter-layer grating coupler has a peak efficiency of -6.8 dB at 1533 nm operating wavelength with TE polarization. The demonstrated approach serves as a potential solution for 3D photonic integration and novel 3D photonic devices.

Keywords: Optical Interconnects, Silicon Photonics, Multi-layer, Grating Coupler, Subwavelength Nanostructure, Adhesive bonding

1. INTRODUCTION

As the scaling of microelectronics continues into nanometer range, interconnects becomes the primary limiting factor in Integrated Circuit (IC) performance. Optics, which dominates today's long distance communication, is considered as a promising solution to the demand for low power and high bandwidth interconnects [1]. Polymer optical interconnects and free space optical interconnects have been intensively studied for off-chip interconnects. However, complementary-metal-oxide-semiconductor (CMOS) compatible optical interconnects is preferred for on-chip application. Silicon photonics, which enables monolithic integration of optical interconnects into microelectronic chips, has received worldwide interest for its potential application in on-chip optical interconnects [2]. To date, most silicon photonic devices, including waveguides, couplers and modulators, are demonstrated on the silicon-on-insulator (SOI) platform [3, 4]. However, considering the minimum spacing between optical waveguides to avoid crosstalk, which can not be scaled, and the relatively large sizes of on-chip photonic components, such as low-loss waveguide crossings and beam splitters [5, 6], the bandwidth density (Gbs/ μm) of single-layer silicon photonic chips is limited. Vertical integration of multiple layers of photonic components can ameliorate the limited bandwidth density on a single layer photonic IC, and provide more design flexibility in the system design [7].

Double-layer silicon photonic platforms have been demonstrated with film deposition approaches, including hydrogenated amorphous silicon, polycrystalline silicon and silicon nitride [8-10]. Hydrogenated amorphous silicon deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD) is a low loss material for waveguiding, but sufficient and stable hydrogenation of the silicon dangling bonds is critical to maintain its low loss property. Zhu et al have demonstrated that the propagation loss for hydrogenated amorphous silicon waveguides are sensitive to process temperature and cladding materials [11], and Selvaraja et al have shown that the refractive index change measured from a Mach-Zehnder Interferometer (MZI) starts to occur at 200°C [12]. In addition to thermal stability of hydrogenated

¹ yangzhang@utexas.edu, raychen@uts.cc.utexas.edu; phone 1512 471-4349; fax 1 512 471-8575.

amorphous silicon, another significant challenge is that the charge mobility is very low due to the amorphous structure of the film, thereby limiting its application in high-speed applications. Silicon nitride is another low loss material for waveguiding, but its lower index comparing to silicon increases device footprint, and it also lacks any mechanism for high-speed modulation, limiting nitride to either passive devices or slower devices using the thermo-optic (TO) effect. Polycrystalline silicon waveguides suffers from its high propagation loss, which is due to the scattering and absorption at the grain boundaries. The lowest propagation loss demonstrated for single-mode polycrystalline silicon waveguide is 6.45dB/cm [13], which is much higher than that of crystalline silicon waveguide. Moreover, in order to maximize the grain size of polycrystalline silicon to achieve its low loss property, high temperature (~1000°C) annealing is required [14], which is not compatible with CMOS back-end process.

Single crystalline silicon is the most desirable material for multi-layer silicon PICs due to its superior material properties such as low material absorption loss and high carrier mobility. As it is not currently possible to deposit single crystalline silicon, other approaches have been investigated to build double-layer structures comprised of crystalline silicon, including silicon nanomembrane transfer [15-17] and direct wafer bonding [18, 19]. However, coupling between separated silicon layers has not been demonstrated in the silicon nanomembrane transfer methods. Direct wafer bonding methods, on the other hand, requires high bonding temperature, which is not compatible with CMOS back-end process. Adhesive bonding, which has been used in fabricating nanophotonic devices on silicon nanomembrane [20], serves as a good candidate for fabricating double-layer silicon photonic ICs.

In this paper, we present vertically integrated, double-layer, on-chip, single crystalline silicon nanomembranes as a platform for 3D photonic integration. To validate the possibility of fabricating nano-scale photonic devices on this platform, and fiber-to-chip and inter-layer light coupling, we designed and fabricated fiber-to-chip and inter-layer grating couplers based on subwavelength nanostructures.

2. DESIGN OF GRATING COUPLERS

Figure 1 shows a 3D schematic of our fiber-to-chip grating coupler and inter-layer grating coupler. The two silicon nanomembranes on different layers, which are both 0.25 μm are adhesively bonded by SU-8. The Buried Oxide (BOX) layer has a thickness of 3 μm . The gratings on both layers are formed by periodically patterning parts of silicon layer into subwavelength nanostructures, whose refractive indices can be engineered to accommodate grating coupler design. Such nanostructures provide high coupling efficiency with large optical bandwidth while providing anti-reflection mechanism through destructive interference [21]. Subwavelength nanostructure based gratings can be patterned and etched in the same step with silicon waveguide layer, and thus simplify the fabrication process.

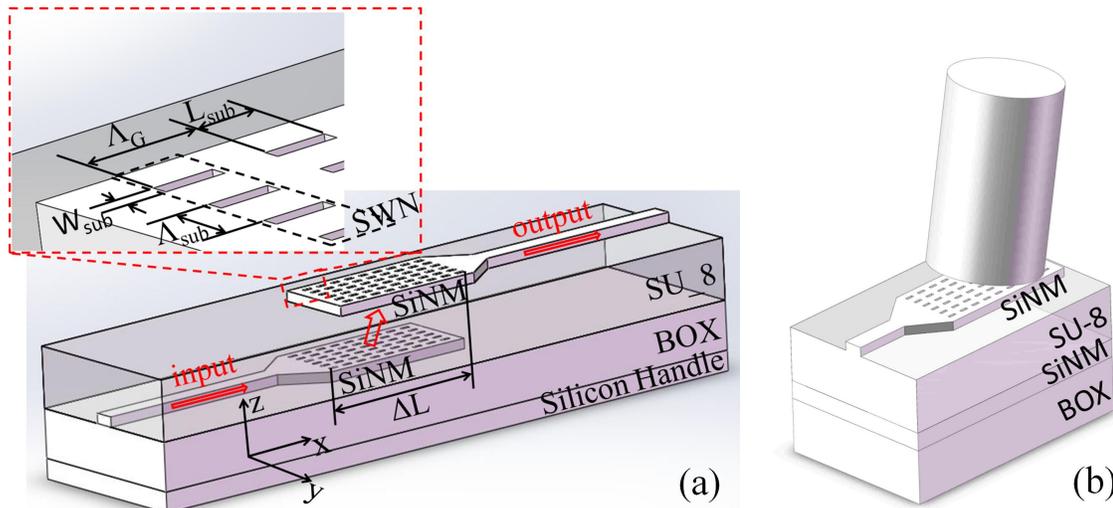


Figure 1. (a) A 3D schematic of the inter-layer grating coupler and subwavelength nanostructure. (b) A 3D schematic of the fiber-to-chip grating coupler. (SiNM denotes silicon nanomembrane, SWN denotes subwavelength nanostructure)

The design of subwavelength nanostructure follows the method described in [21, 22]. Figure 1 shows a schematic of 1D stratified subwavelength nanostructure used in our grating couplers. Silicon and etched rectangular holes are periodically

laminated to form the subwavelength nanostructure. Λ_{sub} is the period of subwavelength nanostructure, W_{sub} is the width of the rectangular etched hole, and L_{sub} is the length of the rectangular etched hole. The refractive index of the subwavelength nanostructure can be calculated using Equation (1) [23]:

$$\frac{\sqrt{n_{\text{si}}^2 - n_{\text{TE}}^2}}{n_{\text{si}}^2} \tan\left(\frac{\pi\sqrt{n_{\text{si}}^2 - n_{\text{TE}}^2}(\Lambda_{\text{sub}} - W_{\text{sub}})}{\lambda}\right) = -\frac{\sqrt{n_{\text{si}}^2 - n_{\text{TE}}^2}}{n_{\text{hole}}^2} \left(\frac{\pi\sqrt{n_{\text{hole}}^2 - n_{\text{TE}}^2}W_{\text{sub}}}{\lambda}\right) \quad (1)$$

Where n_{TE} is the refractive index of subwavelength nanostructure of transverse-electric polarization. n_{si} and n_{hole} are the refractive indices of the silicon and the material in the etched holes, respectively. For the bottom layer, etched holes are filled with SU-8, so $n_{\text{hole}}=1.575$. For the top layer, etched holes are filled with air, so $n_{\text{hole}}=1$. λ is the operating wavelength. Since Equation (1) does not have an explicit analytical solution, we used the second-order polynomial expansion to approximate the tangent function [24]. The refractive index of the subwavelength nanostructure (n_{sub}) can be engineered by tuning W_{sub} with a fixed Λ_{sub} . The grating couplers based on subwavelength nanostructure are treated as conventional grating couplers in the grating coupler design described below, where subwavelength nanostructure is considered as a material with variable refractive index.

The design fiber-to-chip grating coupler follows the method described in [21, 22]. Two-dimensional (2D) finite-difference-time-domain (FDTD) simulations were used to optimize the grating coupler parameters including grating period (Λ_G) and n_{sub} . Grating duty cycle was fixed to be 50%, which corresponds to $L_{\text{sub}}=\Lambda_G/2$. Input light was assumed to be TE polarized. The grating coupling efficiency is also dependent on the thickness of SU-8 layer [22]. However, this thickness was fixed at 3.4 μm in our design because of the fabrication process. We found that the maximum power-upward efficiency is 57% with $\Lambda_G=690$ nm and $n_{\text{sub}}=2.45$ at a power-upward angle of 10° from normal incidence. Figure 2(a) shows the fiber-to-chip grating coupler model in the 2D FDTD simulation. Light is coupled out from the waveguide through the fiber-to-chip grating coupler. The electric field distribution calculated by 2D FDTD with the optimized parameters is shown in Figure 2(a). In order to engineer the subwavelength nanostructure's refractive index to be 2.45, we choose $\Lambda_{\text{sub}}=390$ nm, and the corresponding W_{sub} is calculated to be 80 nm. We used 25 grating periods and 26 subwavelength periods in our grating coupler, which correspond to a grating coupler size of $17 \mu\text{m} \times 10 \mu\text{m}$, to match the mode diameter of standard single-mode fiber (SMF).

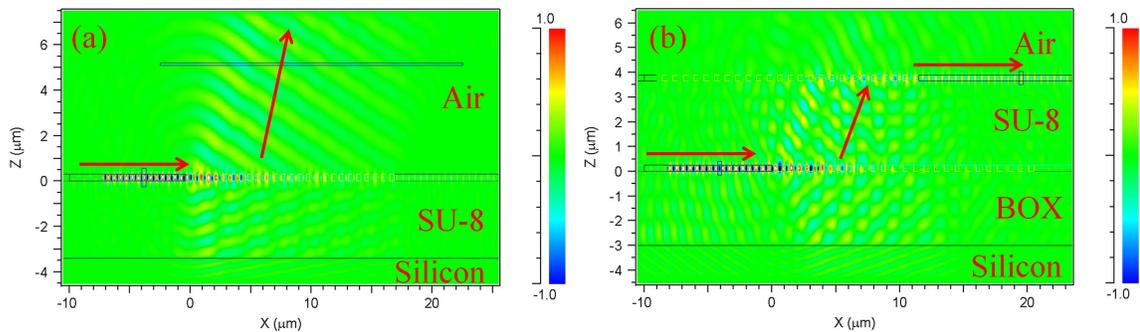


Figure 2. (a) The electric field distribution of the optimized fiber-to-chip grating coupler calculated using 2D FDTD. (b) The electric field distribution of the optimized inter-layer grating coupler calculated using 2D FDTD.

The inter-layer grating coupler consists of two gratings. We used 25 grating periods and 50% grating duty cycle for both gratings. The grating periods (Λ_G) and subwavelength nanostructures' refractive indices (n_{sub}) for both gratings were chosen to be the same. The SU-8 layer thickness is 3.4 μm . Λ_G , n_{sub} and effective length (ΔL), which is defined as the distance between the start of the grating on bottom layer and the end of the grating on top layer, were optimized by 2D FDTD simulations. The input light is assumed to be TE polarized. We found that the maximum coupling efficiency of the inter-layer grating coupler is 21% at 1530 nm operating wavelength with $\Lambda_G=820$ nm, $n_{\text{sub}}=2.5$ and $\Delta L=11.5 \mu\text{m}$. We used $\Lambda_{\text{sub}}=390$ nm for the subwavelength nanostructures of both gratings. W_{sub} of grating 2 was calculated to be 141 nm with $n_{\text{hole}}=1.575$, $n_{\text{sub}}=2.5$ and $\lambda=1530$ nm. W_{sub} of grating 3 was calculated to be 75 nm with $n_{\text{hole}}=1$, $n_{\text{sub}}=2.5$ and $\lambda=1530$ nm. Figure 2(b) shows the fiber-to-chip grating coupler model in the 2D FDTD simulation. Light is coupled out from the waveguide through the fiber-to-chip grating coupler. The electric field distribution calculated by 2D FDTD with the optimized parameters is shown in Figure 2(a). In order to engineer the subwavelength nanostructure's refractive

index to be 2.45, we choose $\Lambda_{\text{sub}}=390$ nm, and the corresponding W_{sub} is calculated to be 80 nm. We used 25 grating periods and 26 subwavelength periods for gratings on both layers, which correspond to grating sizes of $20 \mu\text{m} \times 10 \mu\text{m}$.

3. DEVICE FABRICATION

The fabrication process flow of the devices is illustrated in Figure 3. Gratings on the bottom layer were fabricated on an SOI chip (250 nm single crystalline silicon device layer and $3 \mu\text{m}$ BOX layer) using Electron Beam Lithography (EBL) with Zep520A positive e-beam resist and HBr/Cl_2 based Reactive Ion Etching (RIE). This SOI chip served as recipient substrate in adhesive bonding process. Another SOI chip was used as donor substrate in adhesive bonding process (Figure 3(a)). Both chips were cleaned with piranha solution and Buffered Oxide Etch (BOE) before bonding. A five minutes dehydrating bake at 150° were also applied to the chips to ensure high quality SU-8 layers in spinning-on. $\sim 2 \mu\text{m}$ thick SU-8 layers were spun onto both the recipient and donor substrates using SU-8 2002 resist at 3000rpm, followed by a 2 minute pre-bake at 95°C to evaporate the solvent (Figure 3(b)). SU-8 has excellent self-planarization characteristics and low optical loss [25] at the optical communication wavelength range, which make it an ideal adhesive material in our fabrication process. Next, the two substrates were brought in close contact using a home-made chip bonder, which uniformly applied pressure, and kept in a 90°C oven to ensure sufficient reflow of SU-8 for trapped air bubble removal to give high quality bond (Figure 3(c)). After adhesive bonding, the silicon handle of the donor substrate was first polished down to $\sim 100 \mu\text{m}$ thick, and then removed by $\text{SF}_6/\text{C}_4\text{F}_8/\text{Ar}$ based Deep Reactive Ion Etching (DRIE). The BOX layer of the donor substrate served as an etch-stop layer in the DRIE process, and also protected the device layer of the donor substrate before future process. After the silicon handle was removed, the SU-8 layer was exposed to ultraviolet (UV) irradiation through the donor substrate and post-baked for UV induced polymer crosslinking and hardening. The BOX layer of the donor substrate was then removed by wet etching in 49% hydrofluoric acid (Figure 3(d)). This adhesive bonding process results in a SU-8 layer thickness of $3.4 \mu\text{m}$. Finally, gratings were fabricated on the top layer using EBL and RIE (Figure 3(e)).

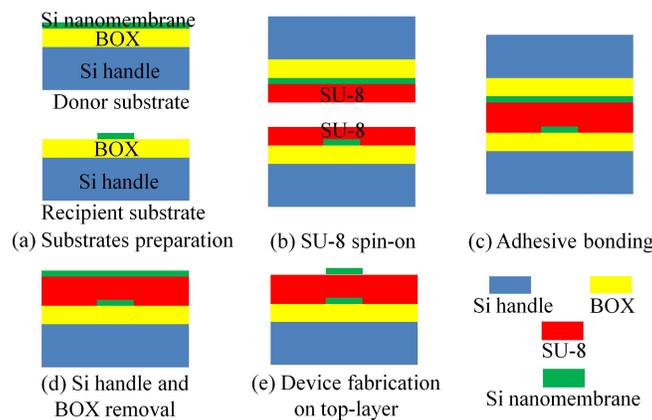


Figure 3. A schematic of the fabrication process flow. (a) Substrates preparation. (b) Spinning-on SU-8 onto substrates. (c) Adhesive bonding. (d) Si handle and BOX removal. (e) Device fabrication on top-layer.

A cross-sectional Scanning Electron Microscopy (SEM) image of the bonded double-layer silicon nanomembranes is shown in Figure 4(a). A SEM image of a fabricated grating on the bottom layer before adhesive bonding is shown in Figure 4(b). Note that the rectangular etched holes on the bottom layer were filled with SU-8 during the bonding process, as shown in Figure 4(c). The alignment between gratings on top and bottom silicon nanomembranes within 100 nm accuracy was realized by electron beam scanning of gold alignmarks on the bottom silicon nanomembrane, which was fabricated on the recipient substrate before fabricating gratings on it.

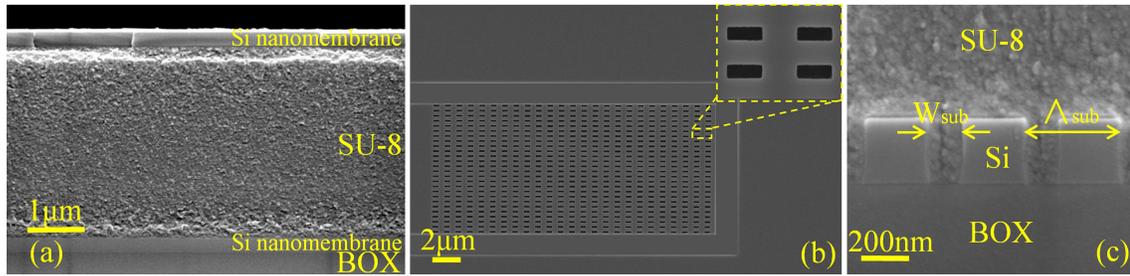


Figure 4. (a) A cross-sectional SEM image of the fabricated double-layer silicon nanomembranes. (b) A SEM image of the fabricated grating 2 before adhesive bonding. (c) A cross-sectional SEM image of the subwavelength nanostructure on the bottom layer showing SU-8 filling the etched holes.

4. DEVICE CHARACTERIZATION

The testing setup is shown in Figure 5(a). TE polarized light from a broad band amplified spontaneous emission (ASE) source is coupled from a polarization maintaining fiber (PMF) with a core diameter of $9\ \mu\text{m}$ to an area-matched linearly tapered waveguide followed by a $2.5\ \mu\text{m}$ wide waveguide on the top layer through a fiber-to-chip grating coupler, and then coupled to a $2.5\ \mu\text{m}$ wide waveguide on the bottom layer through an inter-layer grating coupler. Light propagates within the waveguide on the bottom layer, and then coupled to a $2.5\ \mu\text{m}$ wide waveguide on the top layer through another inter-layer grating coupler. The light is then coupled out to a SMF with a core diameter of $9\ \mu\text{m}$ through another fiber-to-chip grating coupler. The grating regions are connected to $2.5\ \mu\text{m}$ wide waveguides using $500\ \mu\text{m}$ long linear tapers. The final output signal was collected and measured by an Optical Spectrum Analyzer (OSA).

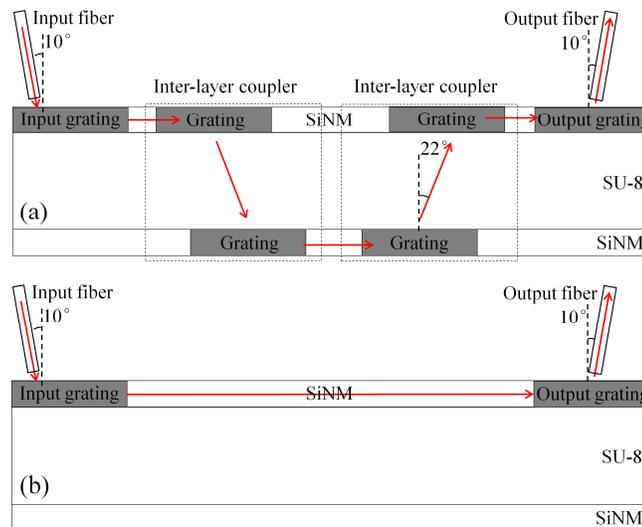


Figure 5. (a) A schematic of the testing setup to measure the efficiency of inter-layer grating coupler. (b) A schematic of the testing setup to measure the efficiency of fiber-to-chip grating coupler, as well as the reference signals for inter-layer grating measurements.

To extract the efficiency of the inter-layer grating coupler from the collected fiber-to-fiber signal (I_1), we used another testing setup to get reference signal, as shown in Figure 5(b). Two fiber-to-chip grating couplers were fabricated on the top layer silicon nanomembrane. Assuming negligible loss from waveguides and linear tapers, by normalizing the collected fiber-to-fiber signal (I_2) to the signal directly from the light source, we first obtained the efficiency of the fiber-to-chip grating coupler, as shown in Figure 6(a). The peak efficiency was measured to be $-3.9\ \text{dB}$ at $1545\ \text{nm}$ wavelength. The efficiency of the inter-layer grating coupler was calculated using $(I_1 - I_2)/2$, as shown in Figure 6(b). The peak efficiency was measured to be $-6.8\ \text{dB}$ at $1533\ \text{nm}$ wavelength. We simulated the efficiency of the inter-layer grating coupler at different wavelengths, as shown in Figure 6(b). The measured loss matched well with our simulated values.

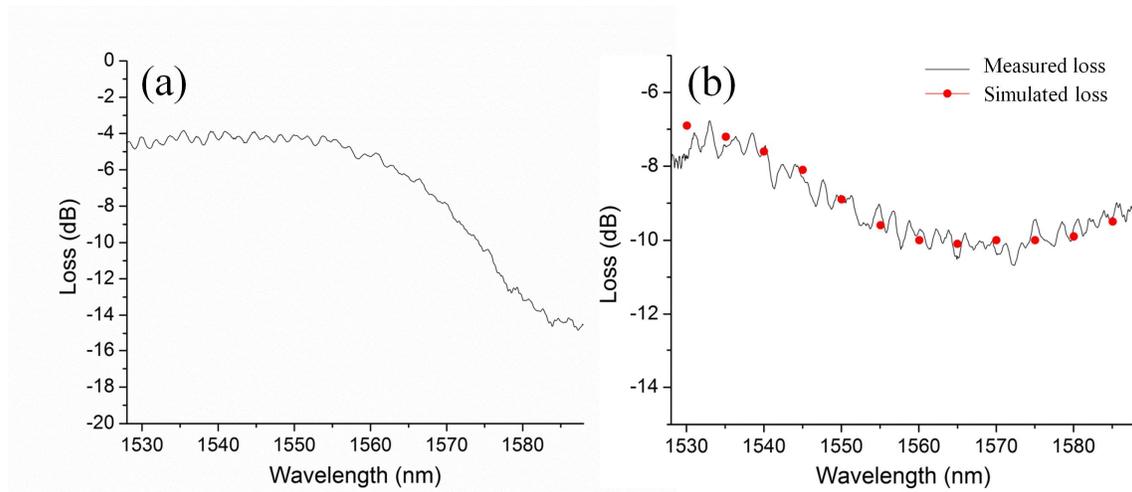


Figure 6. (a) Measured loss of the fiber-to-chip grating coupler. (b) Measured and simulated loss of the inter-layer grating coupler

5. CONCLUSION

In conclusion, we presented a fabrication process flow to fabricate double-layer, on-chip, single crystalline silicon nanomembranes. We demonstrated a fiber-to-chip subwavelength nanostructure based grating coupler on the bonded silicon nanomembrane with a peak efficiency of -3.9 dB at 1545 nm operating wavelength with TE polarization. We also demonstrated an on-chip subwavelength nanostructure based inter-layer grating coupler with a peak efficiency of -6.8 dB at 1533 nm operating wavelength with TE polarization. This approach serves as new platform for three-dimensional (3D) photonic integration and novel 3D photonic devices, such as optical phased arrays (OPAs) [26]

REFERENCES

- [1] Miller, D. A. B., "Device Requirements for Optical Interconnects to Silicon Chips," *Proceedings of IEEE* 97, 1166 (2009).
- [2] Kobrinsky, M. J. Block, A. B. Zheng, J-F. Barnett, B. C. Mohammed, E. Reshotko, M. Robertson, F. List, S. Young, I. and Cadien K., "On-chip Optical Interconnects," *Intel Technology Journal* 8, 129 (2004).
- [3] Lipson M., "Guiding, modulating, and emitting light on silicon-challenges and opportunities," *J. Lightwave Technology* 23, 4222 (2005).
- [4] Anahui, B. Guckenberger, D. Kucharski, D. and Narasimha, A., "A fully integrated 20-Gb/s optoelectronic transceiver implemented in a standard 0.13- μm CMOS SOI technology," *J. Solid-State Circuits* 41, 2945 (2006).
- [5] Bogaerts, W. Dumon, P. Thourhout, D. V. and Baets, R., "Low-loss, low-cross-talk crossings for silicon-on-insulator nanophotonics waveguides," *Opt. Lett.* 32, 2801 (2007).
- [6] Kwong, D. Zhang, Y. Hosseini, A. Liu, Y. and Chen, R.T., "1 X 12 even fanout using multimode interference optical beam splitter on silicon nanomembrane," *Electron. Lett.* 46, 1281 (2010).
- [7] Kash, J. A., "Intrachip Optical Networks for a future supercomputer-on-a-chip," in *Photonics in Switching*, 19-22 August 2007, pp. 55-56.
- [8] Kang, J. Atsumi, Y. Oda, M. Amemiya, T. Nishiyama, N. and Arai, S., "Low-loss amorphous silicon multilayer waveguides vertically stacked on silicon-on-insulator substrate," *Jpn. J. Appl. Phys.* 50, 120208 (2011).
- [9] Preston, K. Schmidt, B. and Lipson, M., "Polysilicon photonic resonators for large-scale 3D integration of optical networks," *Opt. Express* 15, 17283 (2007).
- [10] S-Droz, N. and Lipson, M., "Scalable 3D dense integration of photonics on bulk silicon," *Opt. Express* 19, 17758 (2011).
- [11] Zhu, S. Lo, G. Q. Li, W. and Kwong, D. L., "Effect of cladding layer and subsequent heat treatment on hydrogenated amorphous silicon waveguides," *Opt. Express* 20, 23676 (2012).

- [12] Selvaraja, S. K. Bogaerts, W. Van Thourhout, D. and Schaekers, M., "Thermal trimming and tuning of hydrogenated amorphous silicon nanophotonic devices," *Appl. Phys. Lett.* 97, 071120 (2010).
- [13] Fang, Q. Song, J. F. Tao, S. H. Yu, M. B. Lo, G. Q. and Kwong, D. L., "Low loss (~6.45dB/cm) sub-micron polycrystalline silicon waveguide integrated with efficient SiON waveguide coupler," *Opt. Express* 16, 6425 (2008).
- [14] Kwong, D. Covey, J. Hosseini, A. Zhang, Y. Xu, X. and Chen, R. T., "Ultralow-loss polycrystalline silicon waveguides and high uniformity 1x12 MMI fanout for 3D photonic integration," *Opt. Express* 20, 21722 (2012).
- [15] Xu, X. Subbaraman, H. Hosseini, A. Lin, C. Kwong, D. and Chen, R. T., "Stamp printing of silicon-nanomembrane-based photonic devices onto flexible substrates with a suspended configuration," *Opt. Lett.* 37, 1020 (2012).
- [16] Zablocki, M. J. Sharkawy, A. Ebil, O. and Prather, D. W., "Nanomembrane transfer process for intricate photonic device applications," *Opt. Lett.* 36, 58 (2011).
- [17] Zhang, Y. Carlson, A. Yang, S. Y. Hosseini, A. Kwong, D. Rogers, J. A. and Chen, R. T., "Double-layer photonic devices based on transfer printing of silicon nanomembranes for three-dimensional photonics," in *Conference on Lasers and Electro-Optics*, May 6, 2012, paper CTu1A.
- [18] Zhang, Y. Hosseini, A. Ahn, J. Kwong, D. Fallahazad, B. Tutuc, E. and Chen, R. T., "Vertically integrated double-layer on-chip silicon membranes for 1-to-12 waveguide fanouts," *Appl. Phys. Lett.* 100, 181102 (2012).
- [19] Bauters, J. F. Davenport, M. L. Heck, M. J. R. Doylend, J. K. Chen, A. Fang, A. W. and Bowers, J. E., "Silicon on ultra-low-loss waveguide photonic integration platform," *Opt. Express* 21, 544 (2013).
- [20] Laere, F. V. Roelkens, G. Ayre, M. Schrauwen, J. Tailaert, D. Thourhout, D. V. Krauss, T. F. and Baets, R., "Compact and highly efficient grating couplers between optical fiber and nanophotonic waveguides," *Journal of Lightwave Technology* 25, 151-156 (2007).
- [21] Xu, X. Subbaraman, H. Covey, J. Kwong, D. Hosseini, A. and Chen, R. T. "Complementary metal-oxide-semiconductor compatible high efficiency subwavelength grating couplers for silicon integrated photonics," *Appl. Phys. Lett.* 101, 031109 (2012).
- [22] Subbaraman, H. Xu, X. Covey, J. and Chen, R. T., "Efficient light coupling into in-plane semiconductor nanomembrane photonic devices utilizing a sub-wavelength grating coupler," *Opt. Express* 20, 20659 (2012).
- [23] Yeh, P. Yariv, A. and Hong, C.-S., "Electromagnetic propagation in periodic stratified media. I. General theory," *J. Opt. Soc. Am.* 67 (4), 423 (1977).
- [24] Chen, X. and Tsang, H. K., "Polarization-independent grating couplers for silicon-on-insulator nanophotonic waveguides," *Opt. Lett.* 36, 796 (2011).
- [25] Tung, K. K. Wong, W. H. and Pun, E. Y. B., "Polymeric optical waveguides using direct ultraviolet photolithography process," *Appl. Phys. A: Mater. Sci. Process.* 80, 621 (2005).
- [26] Hosseini, A. Kwong, D. Zhang, Y. Chandorkar, S. A. Crnogorac, F. Carlson, A. Fallah, B. Bank, S. Tutuc, E. Rogers, J. Pease, R. F. W. and Chen, R. T., "On the fabrication of three-dimensional silicon-on-insulator based optical phased array for agile and large angle laser beam steering system," *J. Vac. Sci. Technol. B* 28, C6O1 (2010).