Silicon nanomembrane based compact true-time-delay module on unconventional substrates

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ABSTRACT

We demonstrate several building blocks of true-time-delay (TTD) network, including subwavelength grating couplers, photonic crystal waveguide TTD lines, and multimode interferometer (MMI) power splitters fabricated on silicon nanomembrane (SiNM) transferred onto unconventional substrates, such as glass, Kapton. Bending tests performed on flexible gratings demonstrate operation even at ~15mm bending radius, with about 5dB loss. The 1x16 cascaded multimode interference (MMI) based power splitter demonstrates uniformity of 0.96dB across all the 16 output channels, and an insertion loss of 0.56dB.The photonic crystal waveguides are designed to provide large time delay values within a short length. Photonic crystal tapers are implemented at the strip-photonic crystal waveguide interfaces to minimize loss and provide larger time delay values. A large group index of ~28.5 is calculated from the measurement data, thus indicating achievability of time delay larger than 58ps per millimeter length of the delay line within a tuning range of 20nm. The demonstrated building blocks present a viable path for obtaining scalable TTD modules on unconventional substrates.

Key words: multimode interference, photonic crystal waveguide, true-time-delay, subwavelength grating, silicon nanomembranes, flexible photonics.

1. INTRODUCTION

Advanced military radar systems are increasingly demanding simultaneous multiple beam and wide scanning angle capability, with operation over a broad bandwidth spanning several tens of GHz, which is difficult to realize using traditional electronic phase shifters due to their extremely narrow bandwidth, susceptibility to electromagnetic interference (EMI), and beam squint effect. Processing and transmission of RF signals by photonic systems offers significant advantages to the military systems in terms of data throughput, size, weight, and power (SWaP) requirements, and immunity to EMI [1]. Photonic true-time-delay (TTD) offers better performance with reduced cost, size, weight, and power (C-SWaP) over traditional electronic solutions, especially for simultaneous multi-user, multi-target tracking capability in phased array sensor applications. Several photonic TTD schemes have been proposed to take advantages of an optical feed for TTD, including WDM technique [2-5], slow-light waveguide technique [6], monolithic waveguide technique [7], acousto-optic (AO) integrated circuit technique [8-10], Fourier optical technique [11-13], bulky optics techniques [14-19], Bragg-fiber technique, dispersive fiber technique [20-24], fiber grating technique [25-26], and substrate guided wave techniques [27-29]. Use of photonic systems on air-borne and space-borne platforms or integration of several communication and sensing units on a single chip for improved reliability will require individual components to have smaller size, lower power consumption, and lighter weight. Of the above

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photonic TTD approaches, the fiber-based approach (including dispersive fiber and Bragg fiber based WDM approach) and chip-based approach (including slow-light based approach, and monolithic waveguide approach) have demonstrated great promise for reduced C-SWaP requirements. Since simultaneous receiving/transmission of multiple beams over large steering angles (>±60^o), with operation over wide RF bandwidth is desired, the traditional length scaling approach of the fiber technique will be quite challenging for a photonics chip-based technique. For example, in order to satisfy the beam steering requirements over the wide bandwidth range for a 64 element array, a tunable time delay of ±4.8ns is required, corresponding to a maximum length of 1.0m for a silicon strip waveguide, 2.0m for silica waveguide in a switch based approach, or 66mm of slow-light PCW in a dispersion based approach. Utilizing a silica waveguide configuration, 27m long spirals have been demonstrated [7], which can potentially be used for on-chip TTD units. However, due to the large bending radius required to achieve low loss propagation, each delay arm occupies an area of at least 4cm x 4cm on the chip, which makes it prohibitively expensive for high-bit, high resolution PAA scanning since several delay lines will quickly consume a lot of real estate on the wafers. Moreover, utilization of discrete delay lines on separate chips makes integration unreliable. Our previously demonstrated PCW-TTD structure [6], which occupies only an area of 0.18mm^2 for a 4 delay line configuration, promises extensive miniaturization and integration, with great savings in real estate and potential costs.

Simultaneously, there is a growing demand for developing conformal phased array antenna (PAA) systems that can be mounted on non-planar surfaces, such as on launch vehicles, balloonsonde, and clothing. In order to satisfy the stringent weight and low-profile requirements for these arrays, the feed network needs to be conformal as well. It would be desirable to retain all the unique properties of silicon-on-insulator (SOI)-based TTD [6], but in a light-weight and conformal architecture.

In this paper, we propose an integrated TTD module comprising of SiNM based photonic components. We demonstrate the development of silicon nanomembrane based building block components, such as grating couplers, photonic crystal waveguides, and MMI power splitters, which can be used for developing lightweight, conformal, and compact TTD systems on any substrates. Bending tests show that the devices can be operated well beyond the minimum bending radii of their rigid counterparts, thus making them suitable for conformal PAA system applications.

2. FABRICATION

A home-made bonding tool, as shown in Fig. 1(a), is utilized to first bond a 2cm x 2cm SOI (675 μm handle, 3 μm BOX, 250 nm device layer) onto target (glass and Kapton) substrates. [Note that for membranes transferred onto Kapton substrates, the Kapton is first attached to a glass substrate with an adhesive]. Before bonding, the SOI and target substrate are spin-coated with 5 μm thick SU-8 layer. The native oxide on the surface of SOI is removed with buffered oxide etchant (BOE). The samples are soft baked at 95 ^{o}C to evaporate the solvent. Then, the SOI chip is put upside down on the target substrate and placed in an oven at 65 ^{o}C for 20 mins without applying any pressure. The glass transition temperature of the non-cross-linked SU-8 is 64 ^{o}C, and at the glass transition temperature or above, SU-8 exhibits excellent self-planarization, which minimizes the edge bead effect as well as other thickness variations. Pressure is applied afterwards through the home-made bonder. The material stack is mounted between the two thick

Pyrex glass slides. The steel ball and the Belleville washer spread the point force generated by the thumb screw onto the thick Pyrex glass plate. The pressure is higher at the center than at the edges. This gradient pressure distribution avoids the formation of air cavities in between the two SU-8 layers. As the polymer flows, the pressure decreases, which can be compensated by the thermal expansion of the Belleville washers. The sample is kept in a 65 ^{o}C vacuum oven for 20 hours to allow for polymer to reflow and to squeeze out the trapped air bubbles. After that, the sample is illuminated by 365 nm ultraviolet light through the glass slide to crosslink the SU-8 polymer. Exposure dose is around 150mJ/cm^2. A second long term post exposure bake (PEB) at 65 ^{o}C is done to further crosslink SU-8. After bonding, the silicon handle is removed by deep reactive ion etching (DRIE). To control the thermal budget, the silicon handle is mechanically polished down to ~100 μm prior to DRIE, to shorten the etching time. The inductively coupled plasma (ICP) power and the etching time are carefully tuned to achieve an optimized heat dissipation:etch rate trade-off condition. The silicon etch rate of this recipe is around 2.7 μm/cycle. The 3 μm BOX acts as an etch stop layer, which is later removed by hydrofluoric (HF) acid etching. A picture of the transferred SiNM on glass and Kapton are shown shown in Figs. 1(b) and (c), respectively. The transferred SiNM is examined with an optical microscope, and no visible defects are found.

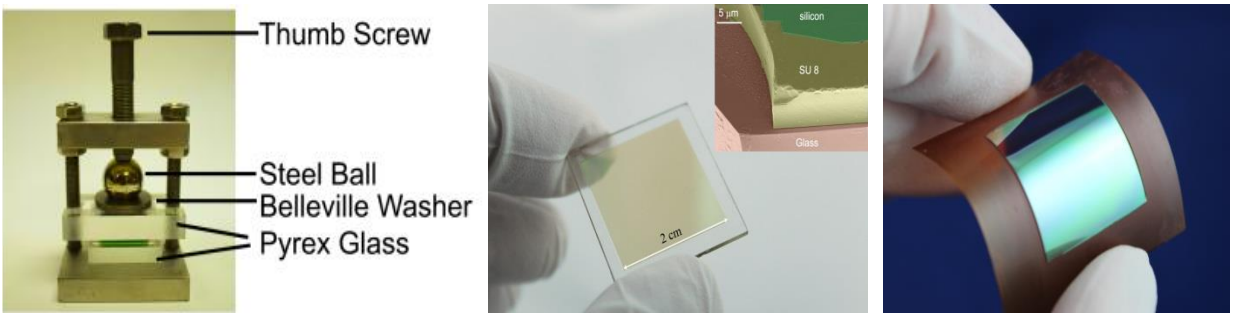

Fig. 1 (a) picture of home-made bonding tool, (b) Microscope image of 2cm x 2cm SiNM transferred on 1mm thick glass substrate. Inset: SEM image of cross section [30], (c) Microscope image of 2cm x 2cm SiNM transferred on flexible Kapton substrate.

The different building block components for the TTD, schematically shown in Fig. 2, are patterned on transferred SiNM using fabrication process described in [31].

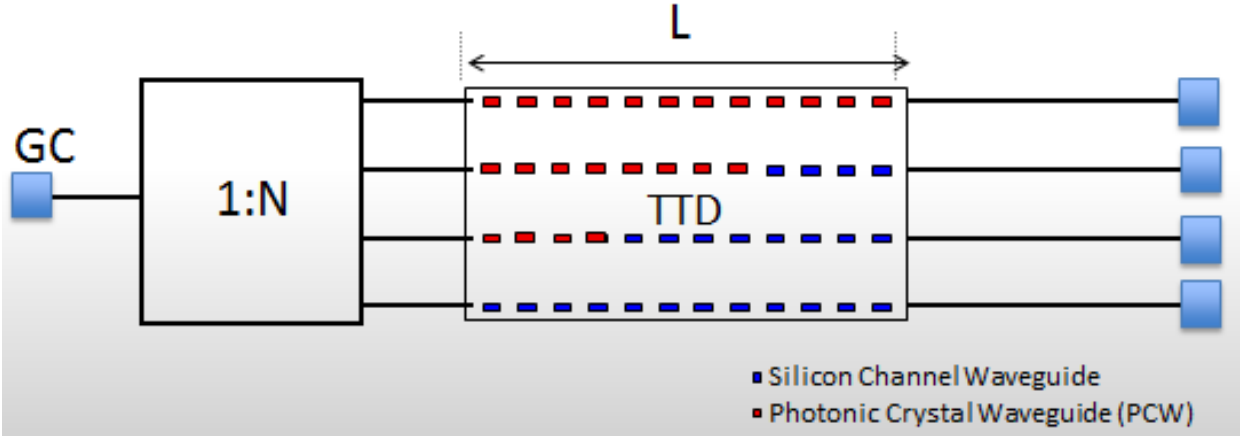

Fig. 2 Schematic of a TTD chip consisting of building block elements: 1) Grating coupler (GC), 2) 1:N MMI power splitter, and 3) Photonic crystal waveguide (PCW) based TTD delay lines

The resist ZEP 520 is first spin-coated on the SOI chip. Next, the resist is patterned with JEOL 6000, and then the patterns are transferred onto the 250nm thick silicon device layer through reactive ion etching (RIE). In this work, the subwavelength grating coupler period, rectangular air trench width,and subwavelength period are chosen to be 0.69μm, 0.090 μm, and 0.39μm, respectively, in order to achieve peak efficiency around 1550nm [32]. For the slow-light photonic crystal waveguide (PCW), period (L) = 405 nm , and a hole diameter (d) = 190 nm are chosen. Photonic crystal tapers are utilized at the strip-PCW interfaces in order to minimize the coupling loss into the PCW, thus enabling operation in the high-group index region near the band-edge, which gives much larger delay time and faster tuning based on wavelength tuning. A 1 × 16 splitter, formed by cascading five 1 × 4 MMIs together, is designed for air (top) and SU-8 (bottom) cladding [30]. A schematic of the optical splitter is provided in Fig. 3.

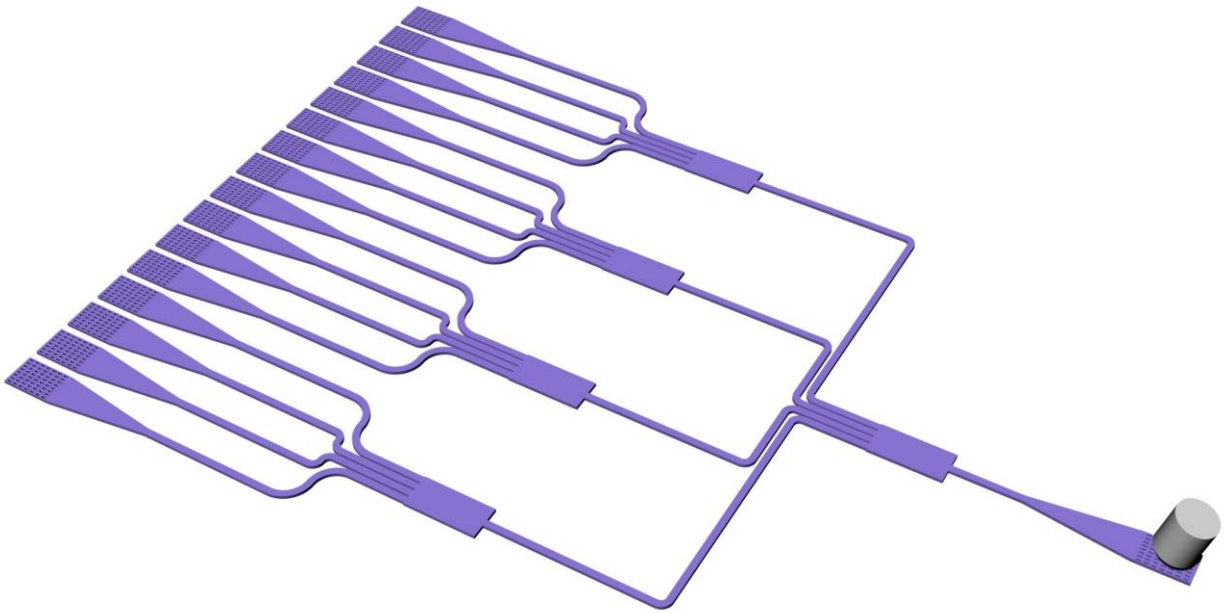

Fig. 3 Schematic of the 1 × 16 optical power splitter composed of two-level cascaded 1 × 16 MMIs [30].

The length and width of the multimode regions are 119.4 μm and 16 μm, respectively. The air holes of the subwavelength structure is 80 × 345 nm. The input and access waveguides are both 2.5 μm wide to ensure low insertion loss and high uniformity [33]. SEM images of the fabricated subwavelength grating coupler, PCW, and the MMI splitter are shown in Fig. 4.

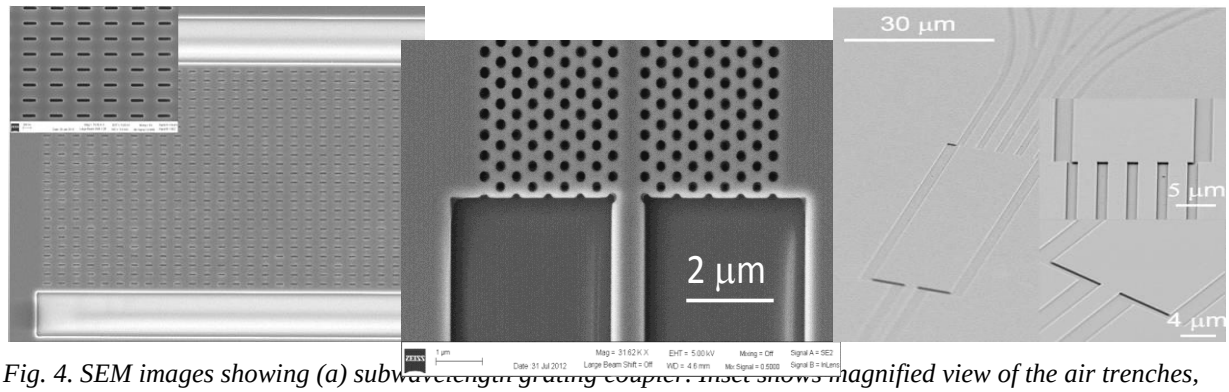

Fig. 4. SEM images showing (a) subwavelength grating coupler. Inset shows magnified view of the air trenches, (b) slow-light photonic crystal waveguide, and (c) a section of the 1x16 MMI power splitter fabricated on SiNM.

3. DEVICE CHARACTERIZATION

We first characterized the bending performance of the fabricated grating couplers. The flexible gratings were mounted between the jaws of a caliper, as shown in Fig. 5. Single mode fibers were utilized to couple light into and out of a pair of grating couples connect via a multimode silicon waveguide.

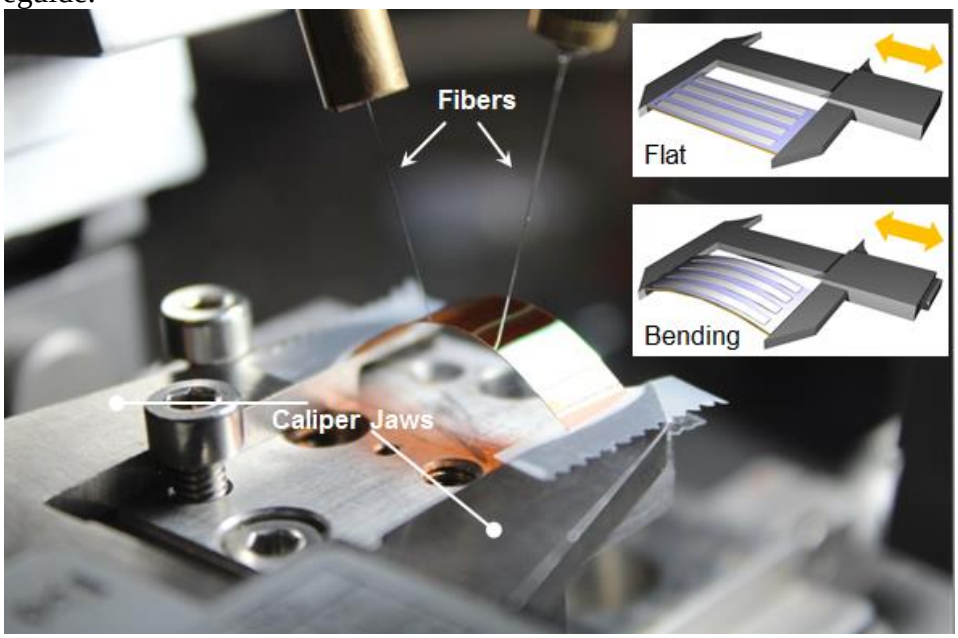

Fig. 5. Experimental setup for measuring the bending performance of SiNM based devices

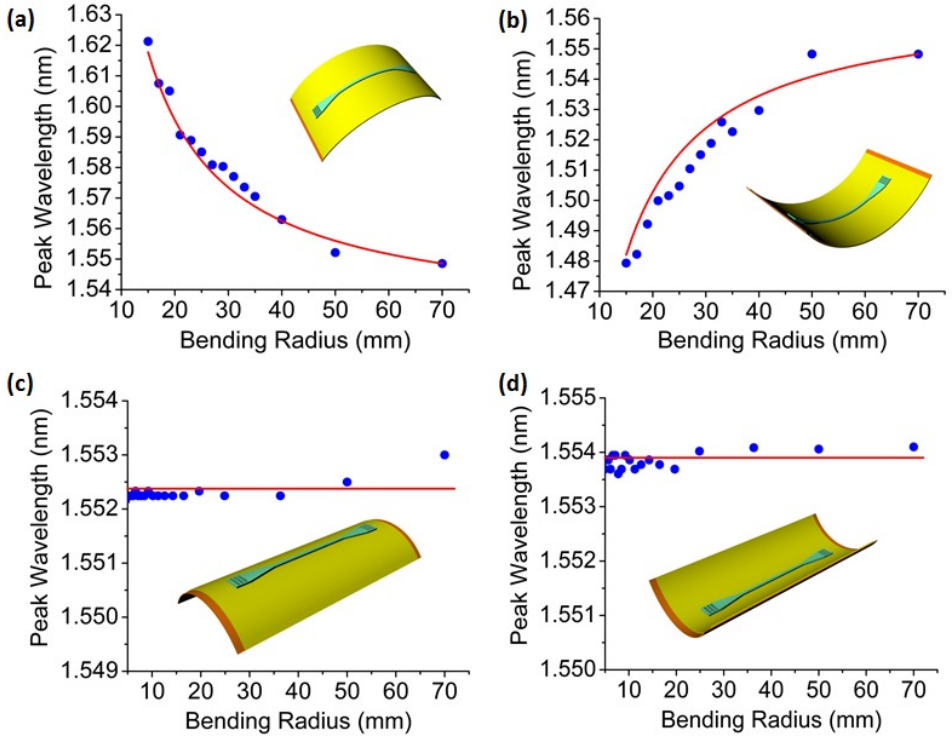

Fig. 6. Bending test results for (a) longitudinal outward bending, (b) longitudinal inward bending, (c) lateral outward bending, and (d) lateral inward bending performed on a pair of SiNM grating couplers

Longitudinal, as well as lateral bending tests, are performed, and the results are shown in Fig. 6. It can be seen from the figure that the measured data (indicated by blue dots) agree well with simulated curves (solid red). Longitudinal bending has a stronger effect on the peak wavelength position than the lateral bending case. Detailed analysis on the bending characterization will be discussed in a future publication. Next the performance of the SiNM based 1x16 power splitter is characterized [30]. The infrared image of the 16 output spots captured by an infrared (IR) camera is shown in Fig. 7. A uniformity of 0.96 dB is obtained at 1545.60 nm, and the insertion loss is measured to be 0.56 dB. The performance is comparable to SOI based MMI splitters [33].

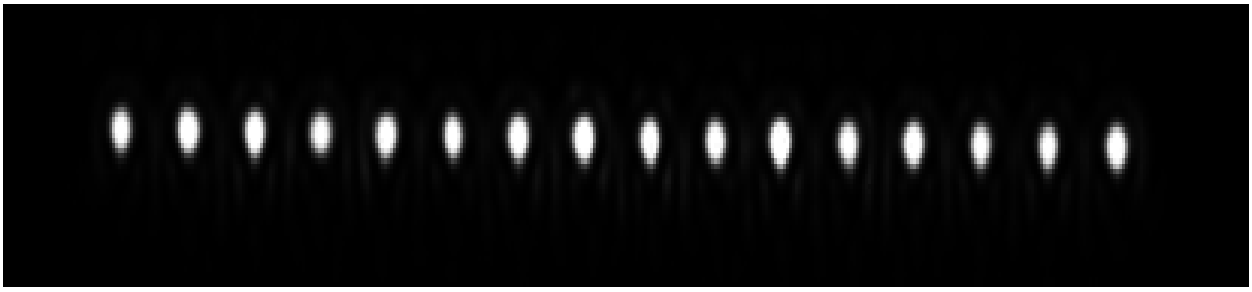

Fig. 7. Infrared image of the 16 output spots from the 1x16 MMI power splitter captured using an IR camera [30]

For the SiNM based TTD lines, using the method outlined in ref [34], we measure the group index of the PCW. TE polarized light from a broadband amplified spontaneous emission (ASE) source is coupled into the SiNM device containing the PCW waveguide via the grating couplers. The input and output fibers are mounted on two 10^{o} wedges, which are mounted on two xyz stages. The input fiber is a polarization maintaining (PM) fiber whose polarization is controlled via a waveplate-based polarization controller (PC). The output fiber is a conventional single mode fiber with a core diameter of 9 μm. The tilt angle can be adjusted from 0^{o} ~ 20^{o}. For this design, both the input and output fibers are tilted ~9.4^{o} from normal incidence. The interference signal between the PCW and the reference arm shows a decreasing fringe spacing as we move closer to the band edge. This is indicative of slow-light effect. From this data, the group index is derived, and shown as red dots in Fig. 8 [35].

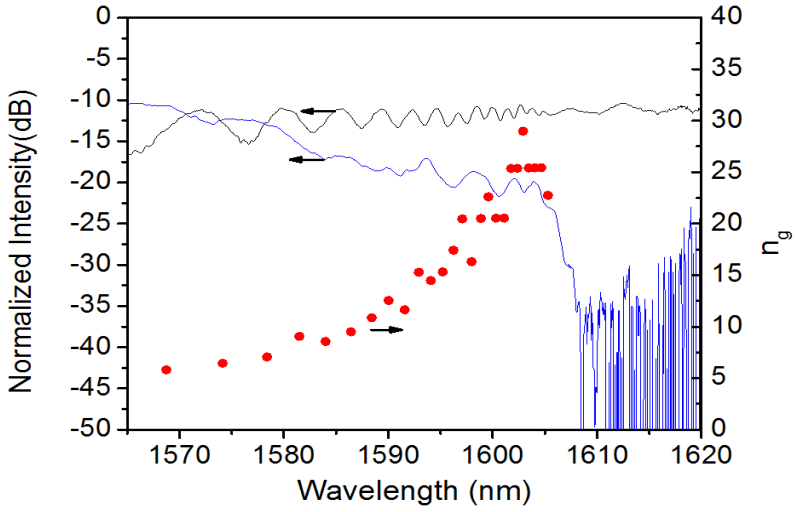

Fig. 8. Measured transmission spectrum from S (blue) and I (black) channels. Calculated group index is shown as red data points [35].

A group index up to 28.5 is measured on the SiNM PCWs. Based on our previous experimental

results [6], wherein a group index of ~23 was obtained from the transferred PCW delay lines, a time delay larger than 216.7ps can be achieved from a 3mm long PCW structure. Thus, using our scheme, we have successfully demonstrated the idea of the development and working of key building block elements required for TTD system. We are currently in the process of developing and testing a full integrated system, and results will be shared in a later conference.

4. CONCLUSION

We have developed a scheme to achieve large area transfer of SiNM onto foreign substrates. To prove the feasibility of development of compact TTD module on any substrate, we first developed and demonstrated key build block components, such as subwavelength grating couplers, slow-light photonic crystal waveguide delay lines, and MMI power splitters, on transferred SiNM. Bending tests are performed, and operation at bending radius as small as 15mm is demonstrated. The insertion losses of grating couplers and 1x16 MMI power splitters are ~ 5dB and 0.56dB, respectively. The uniformity of outputs across the 16 channels of the power splitter is about 0.96dB. The slow-light PCW delay lines show group index up to 28.5. Such slow-light PCWs can enable achievement of time delay values in excess of 58ps per millimeter of PCW. These building blocks can be integrated together to achieve lightweight and conformal compact antenna control systems for air- and space-borne platforms.

5. ACKNOWLEDGMENTS

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