1-to-32 H-tree Optical Distribution on Adhesively Bonded Silicon Nanomembrane

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Abstract: We developed an adhesive bonding process to integrate silicon nanomembranes onto silicon chips. A grating-coupled 1-to-32 H-tree optical distribution is experimentally demonstrated with an excess loss of 2.2 dB and a uniformity of 0.72 dB.
OCIS codes: (230.4170) Multilayers; (230.1360) Beam splitters

1. Introduction

On-chip optical interconnects utilizing silicon platform offers potential benefits compared to conventional metallic interconnects. On-chip optical clock distribution using H-tree structure has been demonstrated on single-layer silicon-on-insulator (SOI) platform [1, 2]. However, it is preferable to stack photonic layers vertically on electronic layers. Comparing to depositable silicon nitride platform [3], single-crystalline silicon nanomembrane offers denser integration density, as well as the possibilities to achieve high-speed photonic integrated circuit (PIC) without using additional layers for active devices.

In this paper, we present the experimental demonstration of a 1-to-32 H-tree optical distribution network on adhesively bonded silicon nanomembranes. The fabricated H-tree structure shows low excess loss, which is comparable to similar structure fabricated on SOI, and uniform outputs.

2. Device design and fabrication

The optical distribution from 1 input to 32 outputs follows H-tree geometry. Each H-tree branch includes 1.1cm single mode waveguides with a cross-sectional dimension of 500 nm X 250 nm, 5-level cascaded compact Y-splitters with an arc radius of 10 μm [4], and three 90° bends with a bending radius of 10 μm. The 32 outputs cover an area of 4 mm X 4 mm, as shown in Fig. 1. In order to perform optical characterization, subwavelength nanostructure based grating couplers described in ref. [5] with 900 μm linear tapers are connected to both input waveguide and output waveguides to couple light in and out of the H-tree structure.

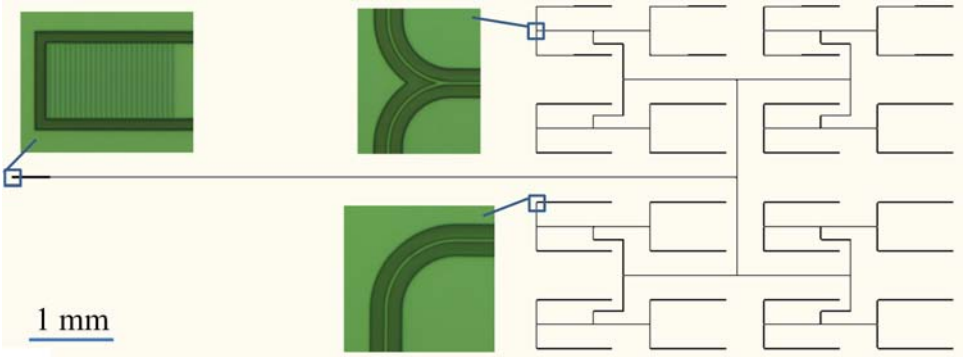

Fig. 1 Schematic of the 1-to-32 H-tree geometry. Optical microscope images of the Y-splitter, the 90° bend, and the subwavelength nanostructure based grating coupler are inserted.

The fabrication process is briefly summarized as follows. Two SOI chips with silicon layers of 250 nm were adhesively bonded using ~3 μm thick SU-8 layer. The silicon handle of top SOI chip was first mechanically polished to ~100 μm thick and then completely removed by deep reactive ion etching (DRIE). A UV exposure and a post exposure bake were done to crosslink the SU-8. After that, the BOX of the top SOI chip was removed by hydrofluoric acid wet etching, leaving a 250 nm thick silicon nanomembrane adhesively bonded to the bottom SOI chip for device fabrication, as shown in Fig. 2(a). ~300 nm thick ZEP-520A positive electronic beam (EB) resist was spun onto the silicon nanommebrane and patterned by EB lithography. A cross-sectional scanning electronic microscope (SEM) image of the resist pattern of subwavelength nanostructure is shown in Fig. 2(b). The resist pattern was then transferred to silicon nanomembrane using HBr/Cl_2 based RIE. Finally, the resist was stripped.

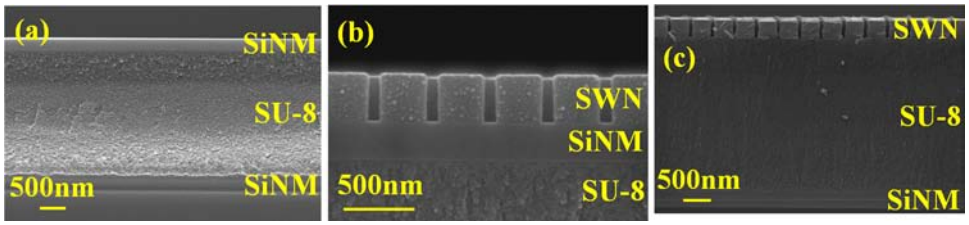

Fig. 2 Cross-sectional SEM images of (a) Adhesively bonded silicon nanomembrane (SiNM), (b) Resist pattern of subwavelength nanostructure (SWN) on bonded silicon nanomembrane, (c) Subwavelength nanostructure on bonded silicon nanomembrane.

3. Device characterization

In order to characterize the total excess loss of the H-tree optical distribution, transverse electric (TE) polarized light was used as the input and a power meter was used to detect the output power from each output at 1550 nm wavelength. The total excess loss, which excludes the fiber-to-waveguide coupling loss and the waveguide propagation loss, is defined as $-\log[(\sum I_m/I_{in})]$, where I_m is the intensity of the m^{th} output channel, and I_{in} is the output intensity of a reference waveguide on the same chip with the same input & output grating couplers and waveguide length as the H-tree structure. The excess loss of the H-tree optical distribution at 1550 nm wavelength is measured to be 2.2 dB, which is mainly from the excess losses of five 1-to-2 Y-splitters. The average excess loss per Y-splitter is 0.44 dB, which is comparable to the results presented in ref. [4].

A top-down IR-image of the entire optical distribution is shown in Fig. 3(a). At each output of the optical distribution, TE polarized light at 1550 nm wavelength was coupled out of the grating coupler and the near field image was collected by an IR CCD camera suspended above the grating coupler. The observation clearly shows 32 outputs. Quantitative measurements of the intensities from each output were performed to characterize the uniformity of this H-tree optical distribution, as shown in Fig. 3(b). The uniformity, which is defined as $10\log(I_{max}/I_{min})$, is calculated to be 0.72 dB.

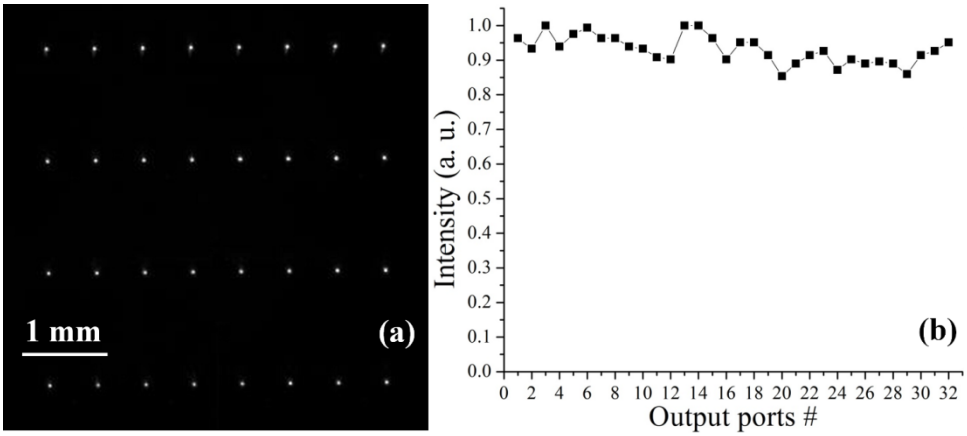

Fig. 3 (a) A top-down IR-image of the 1-to-32 optical distribution, (b) Measured intensities from each outputs of the H-tree structure.

In summary, a 1-to-32 H-tree optical distribution network was fabricated on adhesively bonded silicon nanomembrane. The H-tree structure has an excess loss of 2.2 dB, induced by Y-splitters, and an output uniformity of 0.72 dB. Using the presented method, high-performance optical clock distribution network can be vertically integrated onto existing PICs.

Acknowledgement

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References:

[1] T. Fukazawa, et al, "H-tree-type optical clock signal distribution circuit using a si photonic wire waveguide," Jpn. J. Appl. Phys. 41, 1461-1463 (2002).
[2] L. Vivien, et al, "Experimental demonstration of a low-loss optical H-tree distribution using silicon-on-insulator microwaveguide," Appl. Phys. Lett. 85, 701 (2004).
[3] A. Bibierman, et al, "Optical interconnection networks for high-performance computing systems," Rep. Prog. Phys. 75. 046402 (2012).
[4] S. H. Tao, et al, "Cascaded wide-angle Y-junction 1x16 optical power splitter based on silicon wire waveguides on silicon-on-insulator," Opt. Express 26, 21456-21461 (2006).
[5] Y. Zhang, et al, "On-chip intra- and inter-layer grating couplers for three-dimensional integration of silicon photonics," Appl. Phys. Lett. 102, 211109 (2013).