Vertically Integrated Optical Clock on Adhesively Bonded Silicon Nanomembrane

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***Abstract*—A vertically integrated grating-coupled 1-to-32 H-tree optical clock is experimentally demonstrated on adhesively bonded silicon nanomembrane. This optical clock has an excess loss of 2.2dB, a uniformity of 0.72dB, and a broad transmission spectrum.**

Keywords-Optical clock; silicon nanomembrane; vertical integration

I. INTRODUCTION

Optical interconnects offers potential benefits compared to conventional metallic interconnects in advanced VLSI circuits. On-chip optical clock distribution has been demonstrated on the silicon-on-insulator (SOI) platform [1, 2]. In order to maximize the design flexibility of an optical clock, back-end integration of photonics has been demonstrated to realize 3D integration of photonics on bulk silicon [3, 4], where deposited silicon nitride was used. However, single-crystalline silicon offers the best set of properties for 3D integration of silicon photonics. In this paper, we present the experimental demonstration of a 1-to-32 H-tree optical clock on a single-crystalline silicon nanomembrane. The silicon nanomembrane is adhesively bonded onto a silicon chip to serve as a platform for 3D integration of silicon photonics. By using the presented method, high-performance optical clock distribution networks can be vertically integrated onto existing electronic chips.

II. DEVICE DESIGN AND FABRICATION

The 1-to-32 optical clock distribution follows an H-tree geometry, in which the optical paths are identical for the input to each outputs of the distribution. Strip silicon waveguides with a cross-sectional dimension of 500nm × 250nm are used, which provide stronger light confinement compared to shallow etched rib waveguides. The H-tree geometry includes compact Y-splitters based on arc-shaped branching waveguides [5]. The 32 outputs cover an area of 4mm × 4mm. In order to perform optical characterization, subwavelength nanostructure (SWN) based grating couplers described in [6] with 900μm linear tapers are connected to all input and output waveguides to couple light in and out of the H-tree structure. All output waveguides are folded to align in one direction to simplify alignment between the grating couplers and optical fibers.

The process flow is shown in Fig. 1. Two SOI chips with 250nm thick silicon layers and 3μm BOX layers were first thoroughly cleaned. Next, a 1.5μm thick SU-8 layer was spun onto both the SOI chips, and soft baked at 95°C to evaporate extra solvent (Fig. 1(a)). Then, one SOI chip was put upside down on the other SOI chip. Pressure was applied through a home-made bonder, which is shown in Fig. 1(b). The sample was kept in a 90°C oven for 24 hours to let polymer reflow and squeeze out the trapped air bubbles. The bonded SOI chips are shown in Fig. 1(c). After bonding, the silicon handle of the top SOI chip was mechanically polished down to ~100μm, as shown in Fig. 1(d). This remaining silicon handle was removed by DRIE, as shown in Fig. 1(e). With the selectivity of ~80 for silicon to oxide, the 3μm BOX of the top SOI chip was used as a stopping layer to protect the silicon nanomembrane underneath. After DRIE, the top SOI chip without silicon handle became transparent to ultraviolet light. The sample was illuminated by 365nm ultraviolet light through the top SOI chip to crosslink the SU-8 polymer. A 12-hour post exposure bake at 65°C was done to further crosslink the SU-8. Baking at a low temperature helped minimizing the strain, as the thermal expansion coefficients of silicon and SU-8 are different. After that, the BOX of the top SOI chip was removed by HF wet etching, leaving a 250nm thick silicon nanomembrane adhesively bonded to the bottom SOI chip for device fabrication, as shown in Fig. 1(f). The adhesively bonded silicon nanomembrane can be patterned into the H-tree structures through lithography and etching steps.

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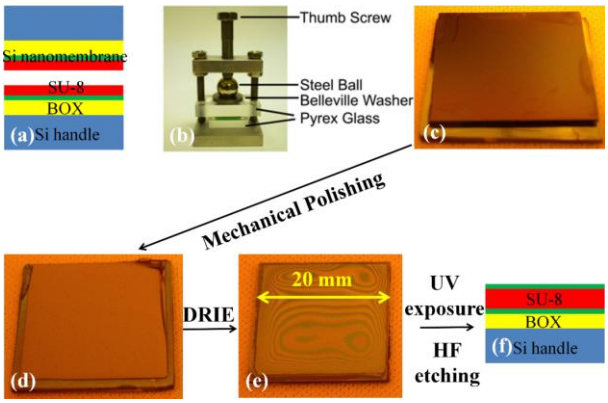

Figure 1. The process flow for bonding silicon nanomembrane onto another SOI chip, (a) schematic of the material stack structure, (b) the home-made bonder used for adhesive bonding, (c) the bonded two SOI chips, (d) polishing the silicon handle to ~100μm, (e) removing the remaining silicon handle with DRIE, (f) schematic of a silicon nanomembrane bonded to a SOI chip.

III. DEVICE CHARACTERIZATION

The propagation loss of strip waveguides fabricated on the adhesively bonded silicon nanomembranes was first measured using the cut-back method. A polarization maintaining fiber (PMF) was used to couple transverse-electric (TE) polarized light at 1550nm wavelength into the waveguides through grating couplers. The output light was collected by a single-mode fiber (SMF) and was measured by an optical power meter. The result is presented in Fig. 2(a). The propagation loss of the single-mode waveguide on the adhesively bonded silicon nanomembrane is 4.3dB/cm at 1550nm wavelength.

In order to characterize the total excess loss of the optical clock, TE polarized light was used as the input, and a power meter was used to detect the output power from each output at 1550 nm wavelength. The total excess loss, which excludes the fiber-to-waveguide coupling loss and the waveguide propagation loss, is defined as $-\log[(\sum I_m)/I_{ref}]$, where I_m is the intensity of the m^{th} output channel, and I_{ref} is the output intensity of a reference waveguide on the same chip with the same input and output grating couplers and waveguide length as the H-tree structure. The excess loss of the H-tree optical distribution at 1550 nm wavelength was measured to be 2.2 dB, which is mainly from the excess losses of five 1-to-2 Y-splitters. The uniformity, which is defined as $10\log(I_{max}/I_{min})$, is calculated to be 0.72 dB.

The transmission spectrum of the optical clock was also characterized. TE polarized light from a broadband amplified spontaneous emission (ASE) source was coupled to the H-tree structure through an input grating coupler, and the output light from one output of the H-tree structure was analyzed by an optical spectrum analyzer (OSA). The transmission spectrum obtained by normalizing the output signal to the light source has a peak value of -29 dB at around 1550 nm wavelength, as shown in Fig. 2(b). This -29 dB includes the coupling loss of two grating couplers, the excess losses, the waveguide propagation loss, and the fanout loss of a 1-to-32 geometry. The two grating couplers' transmission spectrum was obtained by the method described in [6] and is shown in Fig. 2(b). The grating coupler has a peak efficiency of 45% (-3.5 dB) at 1550 nm operating wavelength. Considering the excess loss of five Y-splitters to be 2.2 dB, the waveguide propagation loss to be 4.7 dB (4.3 dB/cm × 1.1 cm), and the fanout loss to be 15 dB, the transmission spectrum agrees well with our previous loss characterizations. We can see that the transmission spectra of grating couplers and H-tree optical distribution have similar profiles through an 80 nm bandwidth, meaning the Y-splitters and waveguide have nearly constant loss in this wide bandwidth.

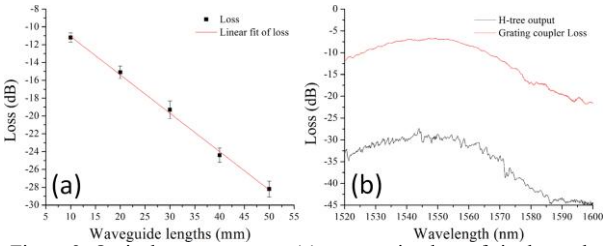

Figure 2. Optical measurements, (a) propagation loss of single-mode waveguide on adhesively bonded silicon nanomembrane determined by varying waveguide lengths using the cut-back method. (b) transmission spectra of the H-tree optical distribution (black) and the two grating couplers for input and output (red).

In summary, a 1-to-32 H-tree optical clock distribution network was fabricated on adhesively bonded silicon nanomembrane. The single-mode waveguides fabricated on this platform has a propagation loss of 4.3dB/cm. The H-tree structure has an excess loss of 2.2dB, induced by Y-splitters, and an output uniformity of 0.72dB.

REFERENCE

[1] T. Fukazawa, A. Sakai and T. Baba, "H-tree-type optical clock signal distribution circuit using a si photonic wire waveguide," Jpn. J. Appl. Phys. 41, 1461-1463 (2002).

[2] L. Vivien, S. Lardenois, D. Pascal, S. Laval, E. Cassan, J. L. Cercus, and A. Koster, "Experimental demonstration of a low-loss optical H-tree distribution using silicon-on-insulator microwaveguide," Appl. Phys. Lett. 85, 701 (2004).

[3] N. Sherwood-Droz, and M. Lipson, "Scalable 3D dense integration of photonics on bulk silicon," Opt. Express 19, 17758-17765 (2011).

[4] A. Bibierman, and K. Bergman, "Optical interconnection networks for high-performance computing systems," Rep. Prog. Phys. 75. 046402 (2012).

[5] S. H. Tao, Q. Fang, J. F. Song, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Cascaded wide-angle Y-junction 1x16 optical power splitter based on silicon wire waveguides on silicon-on-insulator," Opt. Express 26, 21456-21461 (2006).

[6] Y. Zhang, D. Kwong, X. Xu, A. Hosseini, S. Y. Yang, J. A. Rogers, and R. T. Chen, "On-chip intra- and inter-layer grating couplers for three-dimensional integration of silicon photonics," Appl. Phys. Lett. 102, 211109 (2013).