X-Band Printed Phased Array Antennas Using High-Performance CNT/Ion Gel/Ag Transistors

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ABSTRACT

This paper reports a fully printed phased array antenna developed on a 125 micron thick flexible Kapton substrate. Switching for the phase delay lines is accomplished using printed carbon nanotube transistors with ion gel dielectric layers. Design of each element of the phased array antenna is reported, including a low loss constant impedance power divider, a phase shifter network, and patch antenna design. Steering of an X-band PAA operating at 10GHz from 0 degrees to 22.15 degrees is experimentally demonstrated. In order to completely package the array with electrical interconnects, a single substrate interconnect scheme is also investigated.

Keywords: inkjet printing, phased array antenna, carbon nanotubes, printed electronics, X-band, printed transistor

1. INTRODUCTION

In recent years, printed electronics has quickly emerged as an area of great interest in device manufacturing. Based on its compatibility with flexible substrates suitable for wearable and/or conformable devices and high throughput of roll-to-roll (R2R) methodologies[1], printed electronics has the potential to open doors to new types of nano- and micro-device paradigms.

One group of devices that is particularly well suited to current printed electronics technology are conformal, large-area phased array antennas (PAAs). A PAA system implements a moving-parts-free RF beam steering with large field of view and better control of directionality. These systems are heavily used in air-borne and space-borne applications, as they tend to have greater range and better security than omni-directional systems[2]. In a PAA system, directionality is achieved via the constructive or destructive interference of RF signals radiated by an array of identical antennas. By introducing a phase delay between elements, a net directionality is achieved. The antenna themselves do not move, but rather use the phase delays to generate the directionality[3]. In order to achieve a pencil-like beam, a large aperture is required. Compared to conventional fabrication technology, a R2R methodology is a better alternative manufacturing platform for achieving low-cost, light-weight, and conformal characteristics. Additionally, due to a complete printing scheme involved, the challenges of pick-and-place packaging of discrete elements is completely avoided[4].

Compared to our previous demonstration[5,6], in this work, we incorporated high-performance FETs based on fully printed CNT/ion-gel/Ag structure and explore a simple and scalable architecture for electrical interconnect routing. Figure 1(a) shows an in-house developed all-printed PAA operating in the X-band.

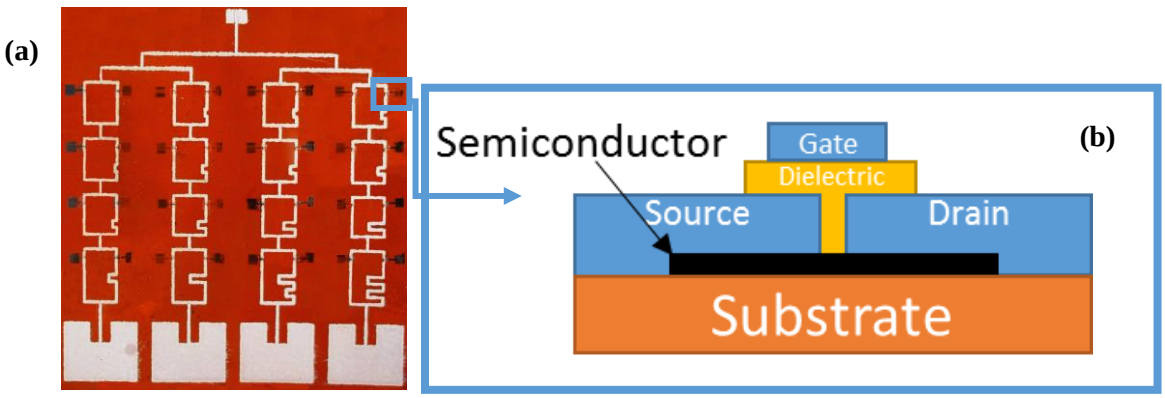

Figure 1: (a) Picture of a 4-bit X-band PAA with 32 CNT-FETs. Each patch antenna is 13.4 mm wide by 11 mm wide. (b) Schematic cross section of layers comprising the CNT-FET switch

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The path that a signal takes to each antenna is controlled via a transistor. The transistors reported in this paper are unique in that they are truly 100% printed devices, using a semiconducting layer consisting of a printed CNT thin film and an Ion Gel dielectric layer. A schematic cross section of the layers forming the CNT transistor switch is shown in Figure 1(b). By controlling the ON and OFF states of the 32 transistors in the 4-bit phase shifter, we are able to demonstrate RF beam steering from our 4-bit, 1x4 PAA device.

The paper is organized in the following order. Section 2 covers the design aspects of the important modules forming the PAA system. In Section 3, the fabrication procedure for developing the PAA is discussed. In order to achieve complete packaging of the PAA, an interconnect scheme based on printed 'vias' is introduced. In Section 4, the characterization and analysis results for the different fabricated structures is presented. Finally, concluding remarks are provided in Section 5.

2. PHASED ARRAY ANTENNA DESIGN

Our designed PAA consists of three major modules, namely, the phase shifter, transistors for controlling flow to the different delay lines, and an array of patch antennas, as highlighted in Figure 2. In this section, aspects of designing these modules is presented.

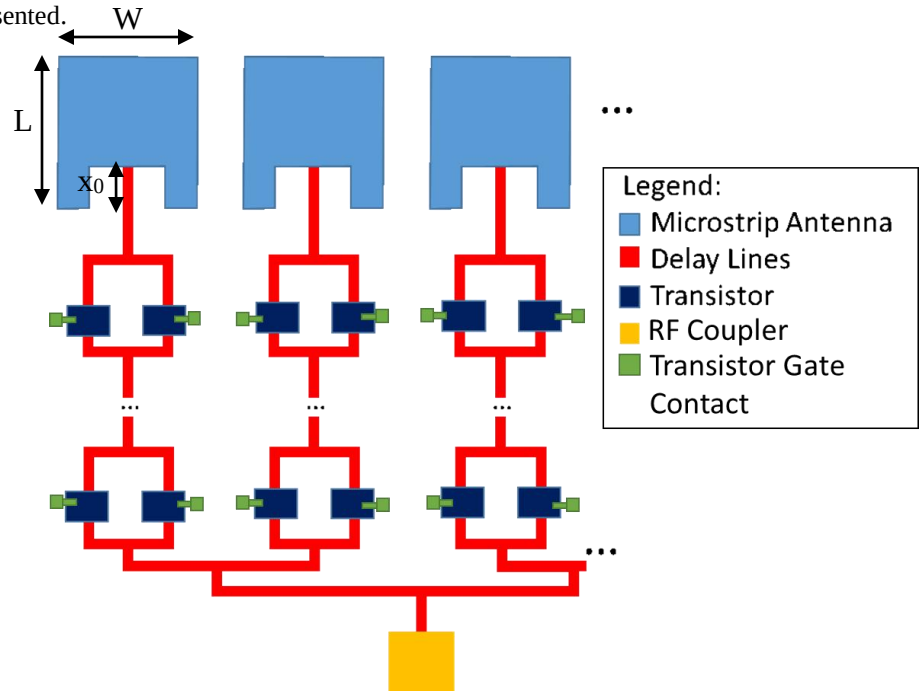


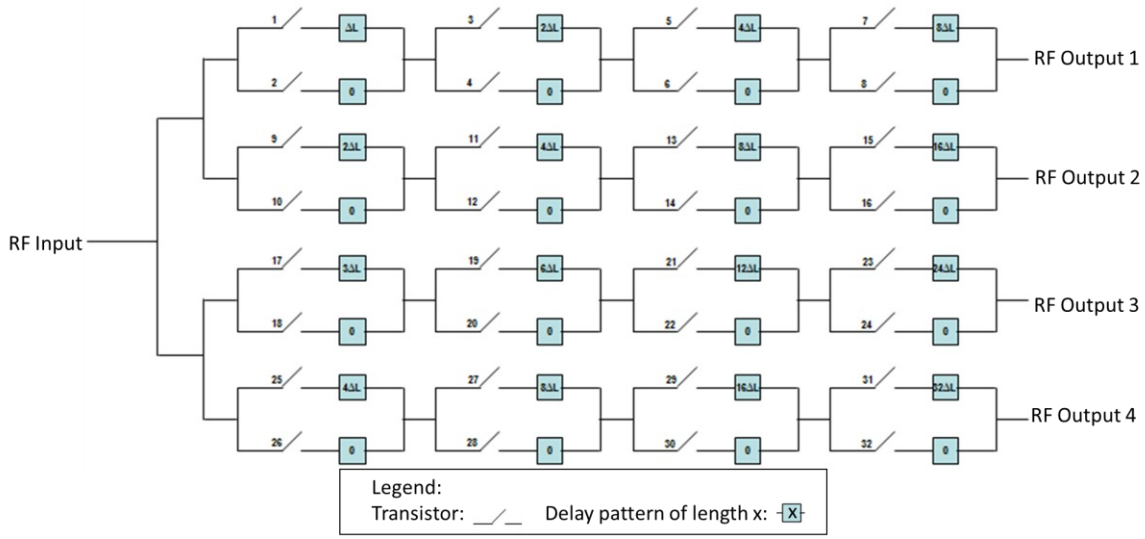
Figure 2: Schematic of a phased array antenna system. The different modules that form the PAA are also shown. Note that only a 1D array is shown for clarity.

2.1 Phase Shifting

In order to achieve the beam steering, the signal for each PAA is run through transmission lines with different lengths. Depending on the relationship between these different lengths, different degrees of beam steering will be achieved[7]. These transmission lines are laid out as a metallic waveguides using the silver ink.

The general layout of the 4-bit (2^4) 1x4 phase shifter is shown in Figure 3(a). We define a minimum path length step as ΔL. This minimum ΔL determines the smallest discrete angle that can be scanned using a PAA system utilizing the phase shifters. Switches 1 through 32 are formed using high-performance carbon nanotubes (CNTs) FETs.

By controlling the ON/OFF states of the switches according to table shown in Figure 3(b), an RF beam can be steered from 0 to 45 degrees. The calculated ΔL for an operating frequency of 10GHz for achieving 0 to 45 degrees steering is calculated from basic principles to be 0.216cm.



(a)

S.No	Steering Angle	Path Length Difference	Switch Selection Table
1	0	0	(2, 4, 6, 8) (10, 12, 14, 16) (18, 20, 22, 24) (26, 28, 30, 32)
2	2.7	ΔL	(1, 4, 6, 8) (9, 12, 14, 16) (17, 20, 22, 24) (25, 28, 30, 32)
3	5.4	2ΔL	(2, 3, 6, 8) (10, 11, 14, 16) (18, 19, 22, 24) (26, 27, 30, 32)
4	8.13	3ΔL	(1, 3, 6, 8) (9, 11, 14, 16) (17, 19, 22, 24) (25, 27, 30, 32)
5	10.87	4ΔL	(2, 4, 5, 8) (10, 12, 13, 16) (18, 20, 21, 24) (26, 28, 29, 32)
6	13.63	5ΔL	(1, 4, 5, 8) (9, 12, 13, 16) (17, 20, 21, 24) (25, 28, 29, 32)
7	16.43	6ΔL	(2, 3, 5, 8) (10, 11, 13, 16) (18, 19, 21, 24) (26, 27, 29, 32)
8	19.26	7ΔL	(1, 3, 5, 8) (9, 11, 13, 16) (17, 19, 21, 24) (25, 27, 29, 32)
9	22.15	8ΔL	(2, 4, 6, 7) (10, 12, 14, 15) (18, 20, 22, 23) (26, 28, 30, 31)
10	25.1	9ΔL	(1, 4, 6, 7) (9, 12, 14, 15) (17, 20, 22, 23) (25, 28, 30, 31)
11	28.12	10ΔL	(2, 3, 6, 7) (10, 11, 14, 15) (18, 19, 22, 23) (26, 27, 30, 31)
12	31.23	11ΔL	(1, 3, 6, 7) (9, 11, 14, 15) (17, 19, 22, 23) (25, 27, 30, 31)
13	34.45	12ΔL	(2, 4, 5, 7) (10, 12, 13, 15) (18, 20, 21, 23) (26, 28, 29, 31)
14	37.79	13ΔL	(1, 4, 5, 7) (9, 12, 13, 15) (17, 20, 21, 23) (25, 28, 29, 31)
15	41.3	14ΔL	(2, 3, 5, 7) (10, 11, 13, 15) (18, 19, 21, 23) (26, 27, 29, 31)
16	45	15ΔL	(1, 3, 5, 7) (9, 11, 13, 15) (17, 19, 21, 23) (25, 27, 29, 31)

(b)

Figure 3: (a) Layout schematic of a 4-bit 1x4 phase shifter and (b) Switch selection table for 1x4 phase shifter for 0 to 45 degrees steering.

2.2 Ion Gel Transistor

A printed transistor consists of 4 layers as indicated in Figure 1(b): a source and drain, a semiconducting layer, a dielectric, and a gate electrode. These layers are deposited using printing method on a flexible substrate, such as the Kapton films used in this project.

Active layer of the transistors were printed using an in-house prepared CNT ink consisting of >99% semiconducting single walled carbon nanotubes (SWCNTs), while the source and gate electrodes were printed using a commercially available conductive silver nanoparticle ink. The most unique element of the high-performance transistor design is the use of the ion gel dielectric and the poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) gate. The need for low operating voltage printed electronics working can be satisfied by Electrolyte-gated transistors (EGTs).[8] EGTs with 'ion gel' as the gate dielectric have shown promising characteristics for printed electronics, such as an ON/OFF current ratio of 10^6, a gate-drain current in the nano-Amps range, and more importantly less than 3 volt operating voltages.[9–11] Ion gel is a mixture of triblock copolymer and ionic liquid.[12] Despite micron level thickness, ion gel shows specific capacitance in the order 10 μF/cm^2 which is 10000 times larger than achievable using thin conventional dielectric layer like PMMA, which gives ion gel more printability with current printing methods to relax

the alignment requirements.[13] Moreover, Ion gel capacitance is constant for thickness range of 2-10 µm which also eliminates the thickness control as a challenging step in printing of conventional dielectrics.[14]

The gate electrode is printed using the conductive polymer PEDOT:PSS in order to maximize the performance of the ion gel interactions since silver does not adhere well to the ion gel and exhibits both higher hysteresis and capacitance than the PEDOT:PSS.[15]

2.3 Patch Antenna

For calculating the shape of the patch antennas at the end of the transmission lines, one of the critical values is the effective permittivity of the Kapton. In the past, expected values for this have been approximately 3.5[16]. However, this value assumes no major distortion of the Kapton. When heated to temperatures over 150°C, Kapton shrinks, and the dielectric constant changes markedly. In order to construct antennas at the designed frequency of 10GHz, the permittivity was empirically determined to be 5.4234.

The different dimensions of all the above elements were calculated using standard equations found in literature[4,17]. In the calculations, the thickness values of the Kapton substrate and the printed silver lines were assumed to be 125 microns and 0.4 microns, respectively. The dimensions of the antenna (as shown in Figure 2) are defined as W, L, and x_0, where W is the width of the antenna, L is the length of the antenna, and x_0 is the distance from the edge at which the feed line impedance is 50Ohms. For the 10GHz patch antenna, these were calculated as W = 8.4mm, L = 6.4mm and x_o = 2.4mm.

In order to ensure efficient coupling from a coplanar probe to a printed microstrip transmission line, a coplanar to microstrip converter is required. The converter comprises of a printed coplanar waveguide and a quarter wavelength transition section [18, 19]. Figure 4 shows a schematic showing the different sections of the overall transmission line. Following procedure outlined by Pavlidis and Hartnagel[18], we calculated the parameters for the different sections shown in Figure 4. The calculated values for s3, s2, and w2 in the converter section are found to be 285 microns, 285 microns, and 215 microns, respectively.

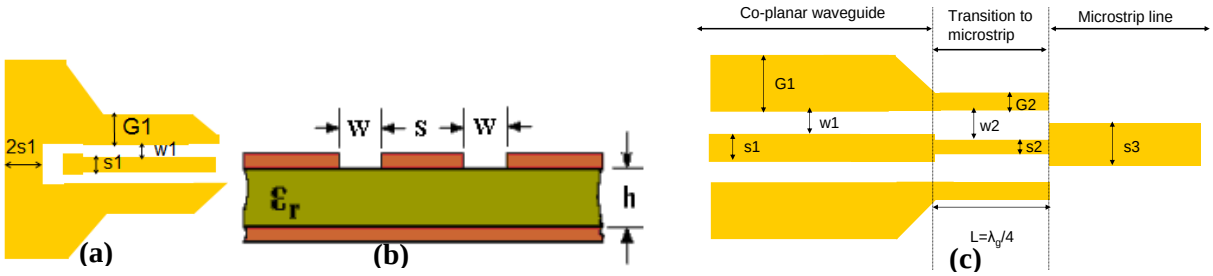


Figure 4: (a) Coplanar waveguide for probing, (b) Microstrip transmission line, and (c) Co-planar waveguide to microstrip line transition.[19]

2.4 Inkjet Printing

Part of what makes the PAA an ideal target for inkjet printing is the fact that with minimal downside, inkjet printing enables light-weight, conformal, and large aperture antennas possible at low cost. As an additive process inkjet printing strictly uses the materials needed only where intended, with minimal waste, and with no requirement for lithographic masks. This allows costs to be reduced providing these antennas at a lower price per unit.

The inkjet printing process consists of three steps, which may be repeated as many times as necessary for the number of layers desired. The first is alignment, in which the position of the print is aligned to the substrate using a fiducial camera built into the system. This alignment is critical as it ensures that each layer is printed correctly relative to the other portions of the device. Typical accuracy for this alignment is +/- 10-20 microns[20]. The second is the print deposition, when the ink is jetted onto the substrate in a thin layer. This may consist of multiple "wet" layers to build up the amount of material on the substrate. Finally, the material is thermally cured, creating adhesion between the layers and the substrate.

3. FABRICATION METHODOLOGY

3.1 Transistor Electrode and Semiconductor Fabrication

The first print layer lays down the source and drain electrodes using a silver nanoparticle ink. This ink is then annealed at 150°C for 30 minutes, which melts the silver nanoparticles into monolithic silver and adheres it to the substrate. Once the electrodes have been established, semiconducting SWCNT ink is printed in the channel regions. The ink is formulated using a mixture of 1-Cyclohexyl-2-pyrrolidone (CHP) and SWCNTs which allows the SWCNTs to be printed using a deposition printer[21]. CHP is ideal for this application, as it has both a relatively low boiling point of 154°C that is stable at room temperature, and a viscosity well suited to use in the Dimatix printing system. The SWCNTs themselves are purchased from Nanointegris, and are delivered as a 99.9% pure powder.[22] This is then mixed with (CHP) at a concentration of 0.2mg of SWCNTs per 10ml of CHP in a sonication bath for 4 hours. Once this process is complete, the resulting mixture can be printed, and then cured at 150°C. The heat causes the CHP to evaporate, leaving the CNTs deposited on the substrate[21]. This process is repeated until the resistance across the channel is finite but very large, indicating an operating SWCNT mesh.

After the solution is deposited on the substrate, the CHP is annealed away by heating to 160 degrees Celsius. Figure 5 shows an SEM image of a CNT thin film after the CHP has been annealed away. The final resistance of the CNT thin film was measured to be 200 kΩ, which was in line with past papers using aerosol printing[23].

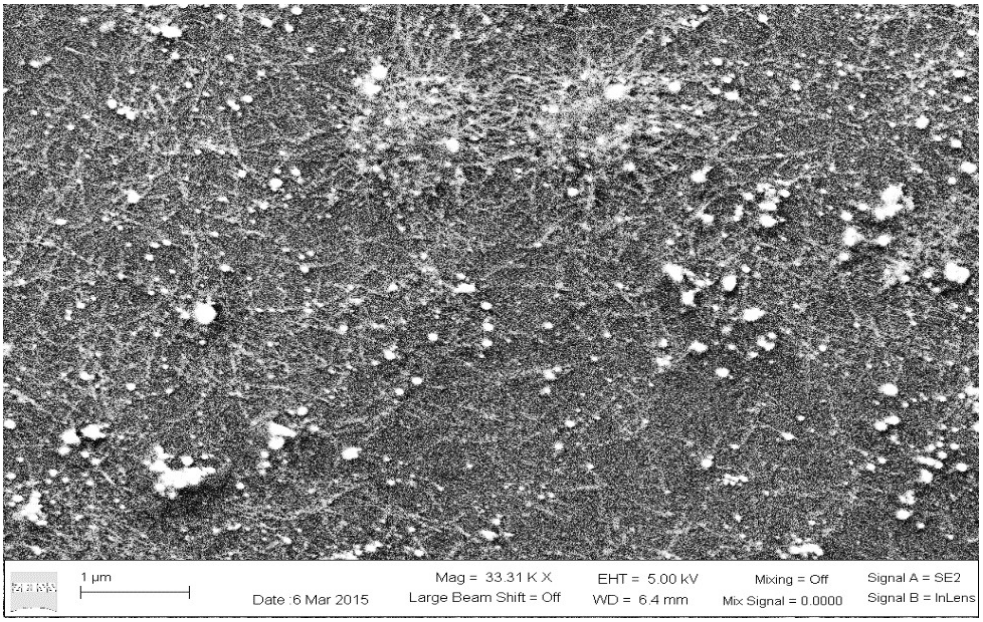


Figure 5: CNT network viewed using a Scanning Electron Microscope at 33000X magnification.

Once the semiconducting Carbon Nanotubes was applied and cured, the integrity of the transistors was verified by checking the resistance across the channel.

3.2 Ion Gel and PEDOT:PSS Materials and Application Process

For the ion gel ink, a solution with the mass ratio of 1/9/90 for poly(styrene-b-methyl methacrylate- b -styrene) (PS-PMMA-PS) /1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)amide [EMI][TFSI]/ethyl acetate was made. The chemical formula and structure for these materials is shown in Figure 6. The (PS-PMMA-PS) polymer was synthesized in-house. [EMMI][TFSI] was purchased from EMD Chemicals. For the poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) ink, PH1000 was purchased from Heraeus, and 6% volume ethylene glycol was added to the ink to enhance the conductivity.

The dielectric (ion gel) and gate (PEDOT:PSS) were sequentially printed by commercial Aerosol Jet Printer (M3D, Optomec Inc). The ion gel layer was printed using 150 µm diameter nozzle size, however, PEDOT:PSS was printed using 100 µm diameter nozzle size. The sheath/feed flow rate for ion gel and PEDOT:PSS were 28/8 and 17/12, respectively.

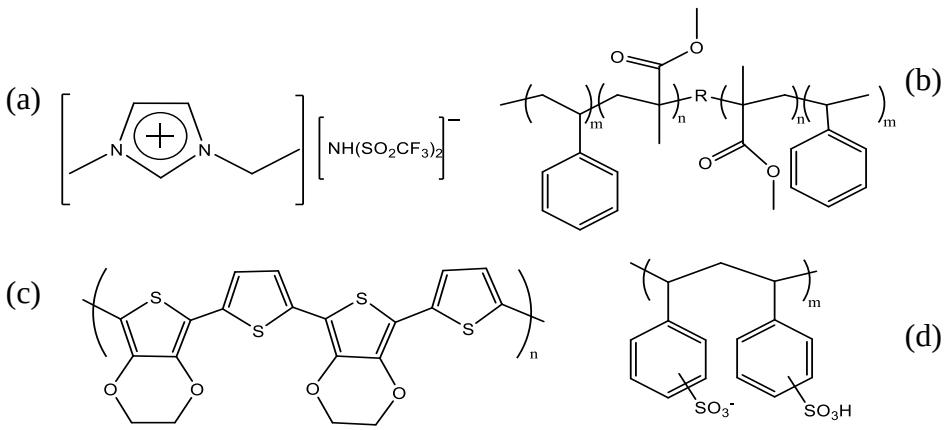


Figure 6: Examples of organic dielectric, conductive materials. (a) [EMI][TFSI] Ionic liquid. (b) SMS, PS-PMMA-PS, triblock copolymer (c) PEDOT (d) PSS. The mixture of (a) and (b), ion gel, is used as dielectric. The mixture of (c) and (d) is a well-documented conducting polymer.

3.3 Single Substrate Interconnects

A multilayer interconnection scheme is required to package a large area, printed phased array antenna system, wherein the signal layout scheme will require the formation of via holes to form 3D interconnects to avoid transmission line path overlaps.

Previously, we developed a multilayer interconnection scheme based on a bonding technique[24], and demonstrated the working of fully packaged 2-bit 1x4 and 4x4 phased array antennas working at 5GHz[25]. The *via* holes required for interconnects were formed by drilling a hole in the top layer prior to bonding. Although straightforward, this bonding technique is difficult to implement for large area circuits, and much more so at high rates in a R2R process. We explored another R2R compatible multilayer interconnection scheme based on a direct-*via* print technique.

The printing process involves printing a bottom conducting layer on a flexible Kapton substrate, followed by a middle insulating layer containing *via* holes, and finally a top conducting layer, which connected to the bottom layer through the *vias*, as shown in Figure 7. A silver nanoparticle ink was used for the conductive layers and SU8-2002 photopolymer was used for the insulating layer. These materials were chosen because they were readily available. However, this technique can be implemented using any printable conductor. Compared to the bonding process, which involved drilling holes in the top substrate, this direct print process directly provides *via* holes in a single step, without the need for any physical drilling processes, thus making them R2R compatible and less complicated.

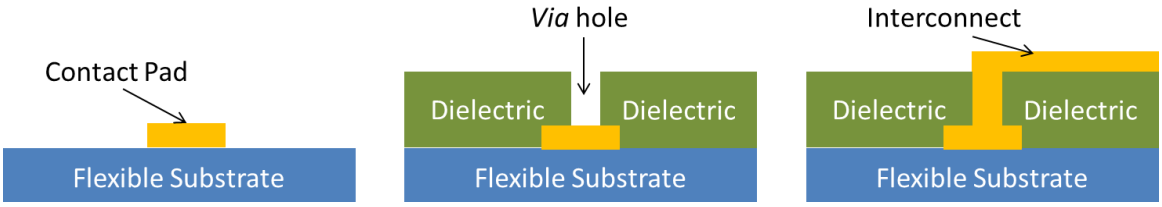


Figure 7: Process flow for developing an ink-jet printed multilayer interconnect

In order to determine the minimum printable *via* hole size, we printed holes of size 20 μm to 180 μm using SU-8, (100 holes of each size), and observed how many were open after printing. The minimum printable hole diameter was 120 μm in the design file, but the printed diameter was between 65 μm and 100 μm due to the viscosity of the SU-8. A zoomed-in microscope image of the printed array of holes with a diameter of 60 microns is shown in Figure 8(a), and a 100% yield of open holes is achieved, thus demonstrating the feasibility of this approach.

A test structure was printed with one *via* hole in the insulating layer connecting a top conductor to a bottom conductor, as shown in Figure 8(b). A digital multimeter was used to measure the resistance of the test structure. The structure was then wrapped around cylindrical rods of different radius, and a multimeter was used to measure the resistance at each bend radius. Finally, a multilayer daisy-chain test structure was constructed to demonstrate continuity through multiple

interconnects, and insulation between unconnected conductors. Figure 8(c) shows the bend resistance resulting from this device structure. It can be seen that a consistent performance is achieved even under bending conditions.

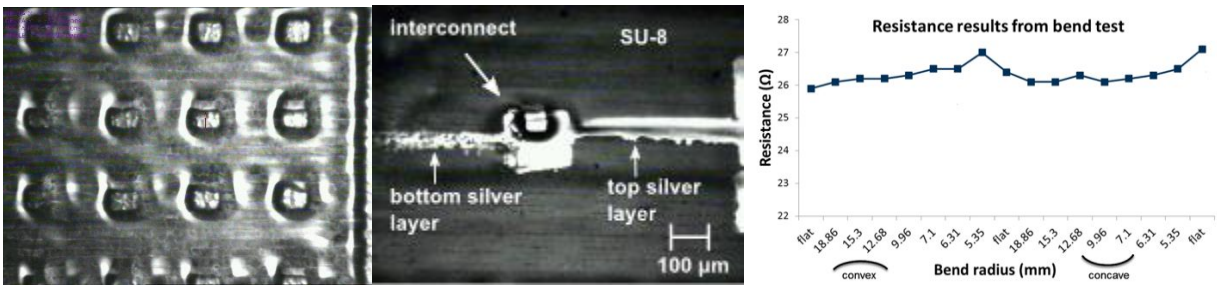


Figure 8: (a) an array of 60 micron holes printed on the substrate showing a 100% yield. (b) Microscope image of a fully ink-jet printed multilayer interconnected test structure, (c) the measured resistance of the test structure as a function of bending radius.

4. EXPERIMENTAL RESULTS

4.1 Single Substrate Interconnect Performance

The measured resistance of the test structur was 34.33 Ω. With an average measured thickness of 0.4 µm[26] we calculated the resistivity to be 4.08 x 10^{-8} Ω.m and the sheet resistance to be 0.10 Ω/square. These values are both well within the range of published specifications for silver ink[26]. However, they can be further improved by optimizing the annealing conditions.

Resistance of the test structure increased with decreasing convex bending radius, as expected, with slight decreases for concave bending. A large increase in resistance was observed in the flat state after concave bending. The increase in resistances were due to silver particles in the via holes being stretched apart, and the decrease in resistance for concave bending (downward bending) was due to the particles being compressed and forming a stronger contact[24].

An additional bend test was performed using a single bend radius of 6.31 mm in order to determine whether resistance would stabilize or continue to increase with repeated bending. Small fluctuations in resistance in the bent positions were observed, but resistance in the flat position stabilized for the last three to five measurements (Figure 9).

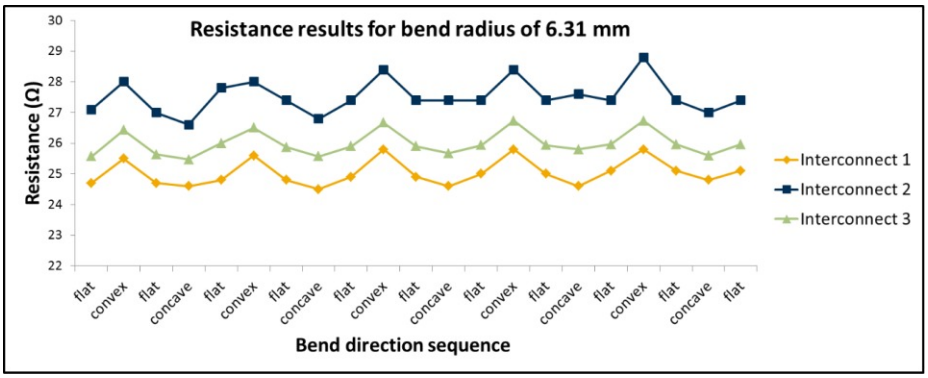


Figure 9: Resistance measurements for the test structure at a bend radius of 6.31mm

The daisy-chain structure successfully demonstrated continuity between interconnected conductors with acceptable resistance, and insulation between unconnected conducting layers.

4.2 Ion Gel Transistor Performance

Prior to incorporating the Ion Gel Transistors in the PAA device, it is important to have a firm grasp on the performance of the individual transistors. This is needed for figuring out properties such as what the gate voltage limitations and performance capabilities of the switching transistor are.

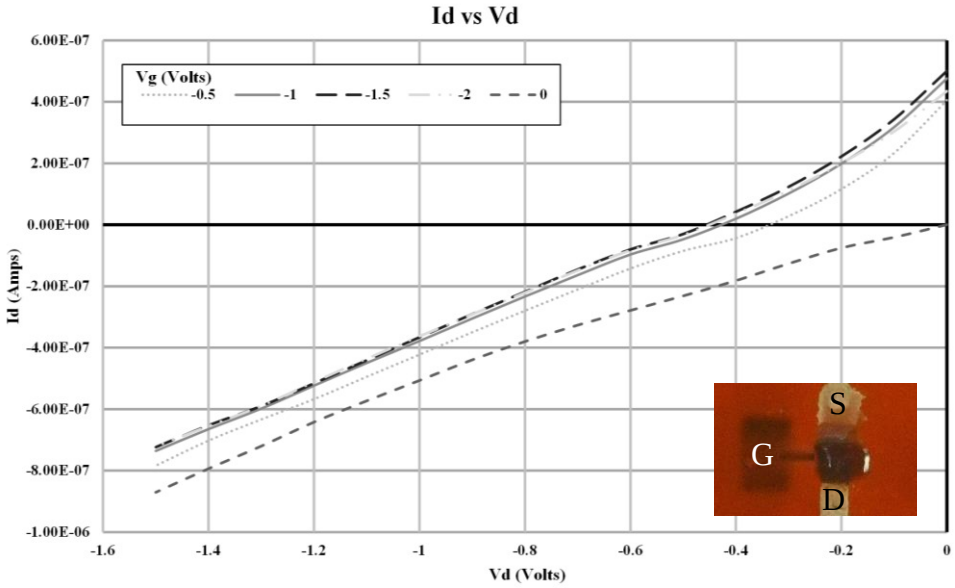


Figure 10: Id vs Vd plot for Ion Gel based printed transistor. A microscope picture of a printed transistor structure is shown on the bottom right.

It is worth noting that there are several environmental limitations on the ion gel devices. Unlike an acrylate dielectric such as a photoresist, ion gel is not environmentally hardened. This means that the maximum gate voltage of the device is limited to +/- 2V, and the maximum temperature is limited to 125°C. This limits the operating range of the device, both in terms of device performance and environmental factors.

First, an Id vs Vd plot was captured using an Agilent B1500A transistor analyzer, which is shown in Figure 10. This determined the range of operating points, and would determine what bias voltages would be tested on the Id vs Vg plot.

Using this Id vs Vd graph as a basis, the operating region of the device could be inferred, and a proper Id vs Vg plot, as shown in Figure 11, could be obtained using the same transistor analyzer.

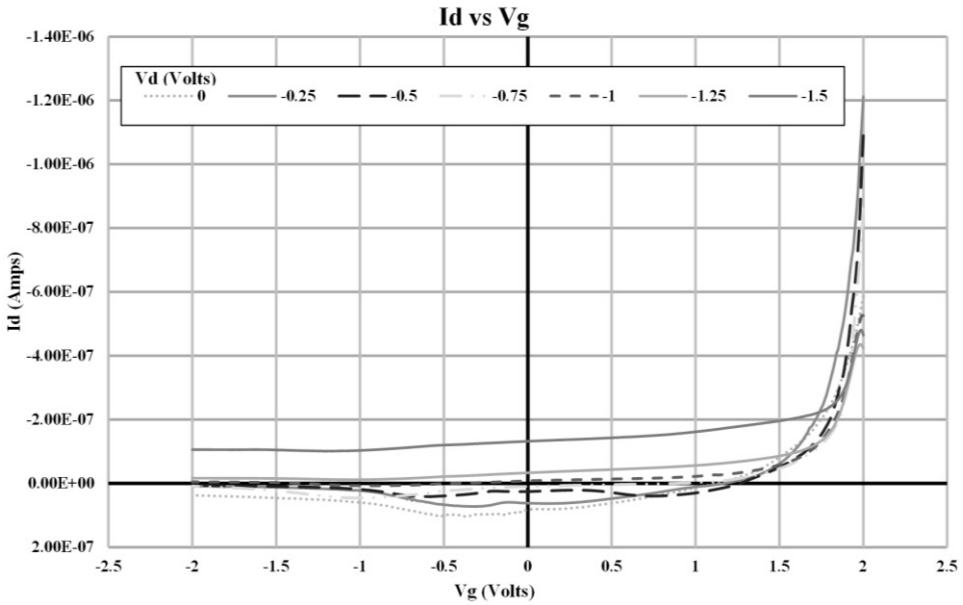


Figure 11: Id vs Vg plot for Ion Gel based printed transistor.

Based on the Id vs Vg plot, we can see that the device has a very good on/off ratio on the order of 10^4. More critically to the overall reproducibility of the ion gel device, the yield rate was relatively high. Prior to assembling the PAAs, groups of 24 transistors were built and tested to verify performance. Across 6 of these transistor sets (a total of 144 transistors) only a single device failed due to a fabrication related error. Additionally, the plots were all significantly similar, leading us to conclude that performance similar to the plots above can be expected for all devices in a PAA.

4.3 Antenna Bandwidth

One of the key properties of conventional PAA devices is that they tend to have very narrow transmitting and receiving bandwidths. In many applications, this is desirable, as it minimizes crosstalk and feedback from other antenna systems. To determine the total bandwidth of the PAA device, an S11 measurement from a network analyzer was used. For this particular sample, the antenna was designed to operate at 10GHz. The plot of the S11 data is shown in Figure 12.

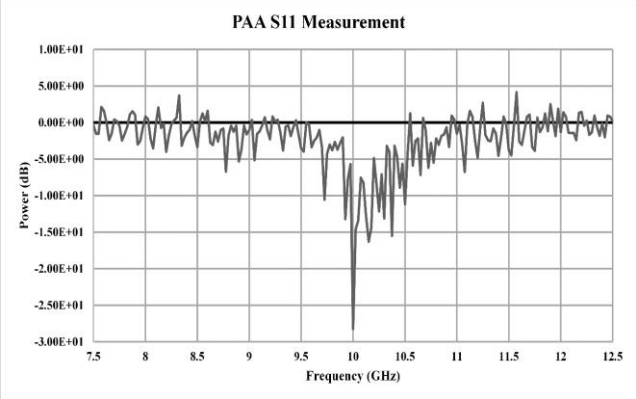


Figure 12: The S11 plot for a 10 GHz PAA device.

As can be seen in the plot, the peak transmission power of the device is at the desired frequency. Furthermore, if we define the bandwidth as the region around the peak above -10dB, we find that this antenna's primary operating range is between 9.975 GHz and 10.075 GHz. This corresponds to a bandwidth of 0.1 GHz, a fairly narrow band as expected for this type of antenna.

4.4 Phased Array Antenna Beam Steering

In order to test the beam steering for the phased array antenna device, it was first necessary to create a test setup which would allow us to get the data. In order to facilitate remote data collection with minimal personnel involvement, an automated test setup was constructed, which is shown in Figure 13.

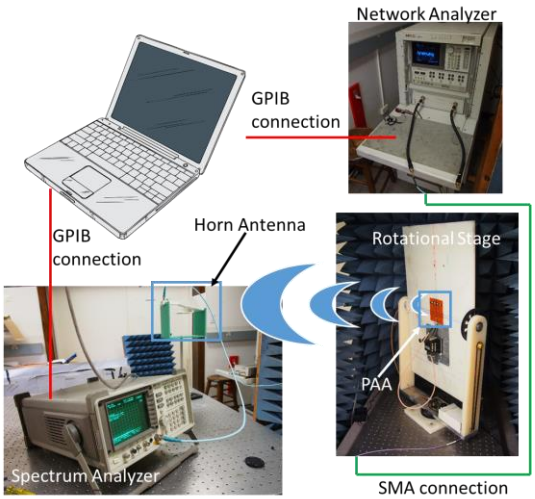


Figure 13: System diagram for the automated test setup.

The automated test setup consists of a rotational stage, with 2 degrees of freedom using stepper motors controlled by an Arduino micro controller, a network analyzer, and a microwave spectrum analyzer connected to a horn antenna shown. A Python program on a computer controls the whole setup. For each measurement, the stage moves to the proper position, uses the network analyzer to generate a signal at a specific frequency which is sent to the PAA, and then records the reading of the horn antenna connected to the MSA. The computer automatically plots the far-field radiation pattern at the end of the scan.

To show the beam steering, the PAA was configured to both a 0 degree and a 22.15 degree configuration, which corresponds to two sets of phase delays generated via switching the individual transistors. These were then plotted next to the modeled theoretical data to ensure that the device was preforming as expected. These results are shown in Figure 14 and Figure 15 for the 0 degree and 22.15 degree PAA, respectively. As we compare the two plots, it is clear that the intended steering effect is being observed.

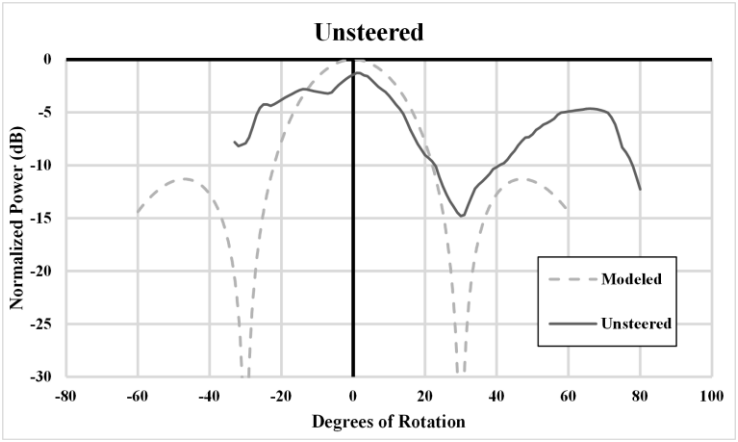


Figure 14: The radiation pattern for an unsteered PAA. The measured data is shown as a solid curve, while the modeled data is shown as a dashed curve.

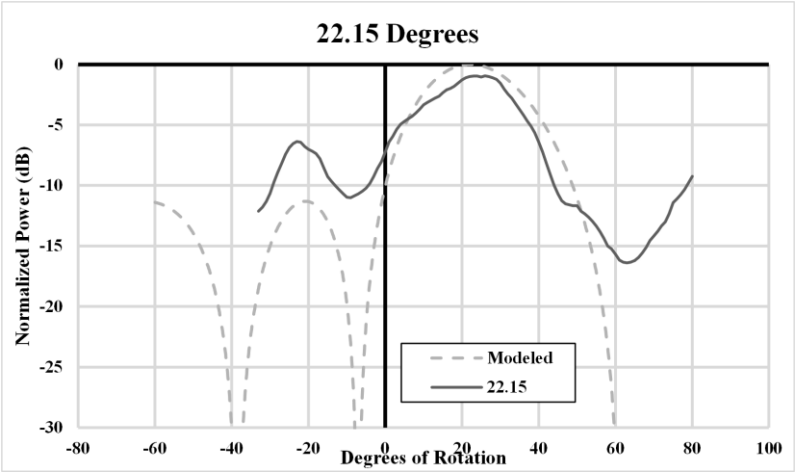


Figure 15: The far-field radiation pattern for a 22.15 degree PAA. The measured data is shown as a solid curve, while the modeled data is shown as a dashed curve.

The shapes of the curves for the measured data closely correspond to the simulated data pattern. However, the peak intensity values do not occur exactly at the exact values. This is due to the fact that the radiation pattern for the 1x4 array is broad, and minor fluctuations in the measured intensity near the peak make it difficult to determine the peak's location. A larger aperture will decrease this uncertainty. The measured side lobes deviate from the simulated curves. This asymmetry is attributed to non-uniform radiation amplitudes of the antenna elements.

5. CONCLUSION

In this paper, we report an X-band Phased Array Antenna which was fabricated using exclusively printing based methodologies. The system consisted of a phase shifting network controlled by SWCNT based transistors. In order to control this packaged device, single substrate interconnects were developed using printed insulating dielectric material with *vias*. The steering capability of the PAA was demonstrated by controlling the ON/OFF states of the 32 transistors, and a beam steering of a 10GHz signal from 0 degrees to 22.14 degrees was experimentally demonstrated. This project represents a unique device in that it is truly 100% printed and takes advantage of the emerging technology of ion gel dielectric materials.

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