Optical Computing on Silicon-on-Insulator-Based Photonic Integrated Circuits

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ABSTRACT

The advancement of photonic integrated circuits (PICs) brings the possibility to accomplish on-chip optical interconnects and computations. Optical computing, as a promising alternative to traditional CMOS computing, has great potential advantages of ultra-high speed and low-power in information processing and communications. In this paper, we survey the current research efforts on optical computing demonstrated on silicon-on-insulator-based PICs. The advantages, limitations, and possible research directions for further investigation are discussed.

1. INTRODUCTION

Optical computing is to use optical systems to perform numerical computations [1]. The idea is to leverage the properties of speed, parallelism and ultra-low power transmission of light in order to process information at a high-data rate. The information can be in the form of an optical signal sourced by optical lasers and detected by photodetectors. In terms of computing, the advantages of the optics include but are not limited to: (1) significant reduction of signal transfer latency, (2) ultra-low energy consumption, and (3) simplified layout architecture for many complex computation structures [2, 3].

In the early days of optical computing, research efforts had focused on free-space optical applications, which includes Fourier transform and pattern recognition [4, 5]. However, these implementations require free space as the medium between transceivers and involve large devices such as lenses, slits or mirrors, which prevent the scaling and integration of free-space applications.

With Moore's law approaching the limits, photonic integrated circuits (PICs) have received increasing attention. Among all platforms of PICs, silicon-on-insulator (SOI) is the most promising due to the CMOS-compatible process enabled low-cost and large-volume manufacturing and the ability of monolithic integration of electronics and photonics. As the footprint of the SOI waveguides and optical devices decreases, nanophotonics also promises the scaling for photonics, similar to the shrinking of CMOS devices [6–9].

Optical logic gates and synthesis have been studied to exploit the aforementioned advantages. Although nonlinear optical devices that directly use light to control light have not been able to meet the low power goals [10], general architectures based on binary decision diagram to allow electrical signals to control light [11, 12] have shown greater potential. Some recent works have also explored the possibility of using optics in specific types of computation such as neural networks, graphical models, Ising models, etc [9, 13, 14].

This paper surveys the emerging representative development in optical computing using SOI-based PIC. Section 2 introduces the common SOI-based optical devices used in optical computing. Section 3 discusses two optical computing paradigms, logic functions and matrix multiplication, both of which can be realized in SOI-based PIC. The advantages and limitations are also studied. The paper is concluded in Section 4.

2. OPTICAL COMPUTING COMPONENTS

In this section, we introduce the common SOI-based optical components that demonstrate computing capabilities as well as their working principles.

2.1 Mach-Zehnder Interferometer

The Mach-Zehnder interferometer (MZI) is a common integrated photonic device used as electro-optic modulators and switches. In the 2×2 MZI in Figure 1a, the lights from input ports a, b go into a splitter, traveling for some distance, then are combined to the output a', b'. MZI demonstrates constructive/destructive interference in the combiner depending on the phase difference $\Delta\phi$ of the two paths and leads to a frequency-dependent response in the amplitude of the output. The phase difference can be expressed as $\Delta\phi = 2\pi/\lambda \cdot \Delta N_{eff} \cdot L$, where λ is the operating wavelength, N_{eff} is the effective refractive index of propagating mode of the waveguide, L is the length of the sensitive arm.

When the phase $\Delta\phi$ is set to π such that the combined lights have opposite phase difference and there is no light at the output port. If this phase shift $\Delta\phi$ is controlled by an electrical signal (by changing N_{eff}), the MZI implements an electrical-optical (EO) switch.

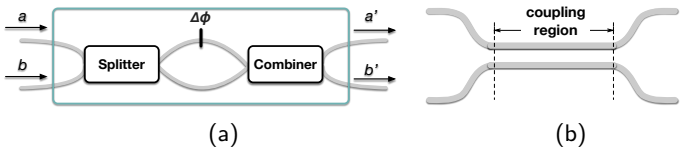

Figure 1: (a) Mach-Zehnder Interferometer. (b) 2×2 Directional coupler.

2.2 Microresonators

Like MZIs, microresonators, such as microrings and microdisks can also be used to realize modulation and switching. Figure 2a shows a schematic of a typical 2×2 microresonator-based optical switch/modulator using microrings, which has a light input and two outputs: the through output and drop output. When a continuous wave (CW) light is fed into the switch from the input, part of the light is coupled into the microresonator, and then coupled back to the two bus waveguides with certain phase shifts. This results in a wavelength selective behavior shown in the black curves of Figure 2b. One could apply an electrical signal to shift the resonance peaks to switch the light, which is illustrated with the red and blue curves. By using both the through and drop ports of the switch, one can build optical switches controlled by electrical signals. The light

passes or terminates depending on the controlling electrical signal.

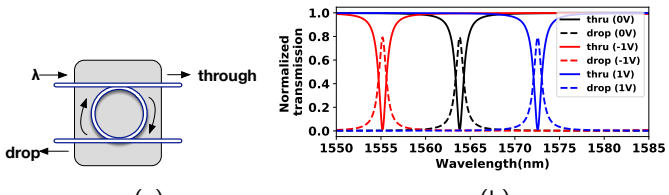

Figure 2: (a) Schematic diagram of a microresonator (b) 2×1 and 1×1 switch notations (c) Optical transmission spectra measured at through and drop ports under various bias.

Table 1 shows a comparison of EO switches using MZI, microring and microdisk [15–17]. Compared with MZIs used in the previous work, microresonators such as microrings and microdisks, have much a smaller footprint. The microresonators are used in microresonator-based optical switches that could be driven by a CMOS-compatible voltage ($< 1Vpp$) with much lower energy consumption($< 50fJ/bit$).

Table 1: Comparison of EO switches.

	MZI	Microring	Microdisk
Footprint	$\sim 2000 \times 500um^2$	$\sim 10 \times 10um^2$	$\sim 5 \times 5um^2$
Insertion loss	~2.2 dB	~2.8 dB	~0.9 dB
Extinction ratio	~4.1 dB	~6.6 dB	~7.8 dB
Energy	~750 fJ/bit	~50 fJ/bit	~1 fJ/bit

2.3 Directional Coupler

The directional optical coupler (Figure 1b) is a guided wave component for combining/ splitting lights with a controllable combining/splitting ratio, which is decided by the coupling efficiency. Coupling occurs when two waveguides are brought within close proximity to each other such that the electromagnetic fields in one waveguide extend over the other waveguide and vice versa, causing energy to cross over between one waveguide to the other, as a function of coupling length.

The coupling efficiency is adjustable in the range of 0 to 100% by adjusting the coupling length, which provides further computational capabilities compared with plain Y-branch combiner/splitters. An $N \times 1$ coupler can be obtained by cascading (N-1) 2×1 couplers, with an arbitrary coupling efficiency to each input.

3. COMPUTING PARADIGMS

In this section, we will discuss two representative optical computing paradigms, one for general optical logic gates and logic function synthesis, and the other for linear optics based optical computing, such as matrix multiplication and the neural network application.

3.1 Logic Gates and Synthesis

A majority of previous works on digital optical computing have been focusing on basic Boolean operations such as (N)AND, (N)OR and X(N)OR gates [18–20] and relatively more complex functionalities such as 1-bit half and full adders [3, 21].

More recently, in order to implement general and large-scale PICs and pave the way for design-space exploration, general logic synthesis methods have been studied. A synthesis scheme based on virtual gates (VGs) and optical splitters were proposed in [22]. A virtual gate is a 2×2 crossbar that could be switched by a function, not necessarily a primary input. In that work, each literal of a boolean function is implemented by a VG. While the concept of such virtual gates is worthwhile for functional cascading, the proposed method usually generate a large number of optical components, such as VGs and splitters.

A straightforward binary decision diagram (BDD)-based synthesis method [11] is shown in Figure 3. BDD [23] is a widely used data structure for logic synthesis and verification. Each decision node in a BDD has a function of a 1×2 crossbar switch, which is controlled by a decision variable. The switch can be implemented with either MZIs or microresonators. In optical synthesis, the 1-terminal node of a BDD is connected to a photo-detector, corresponding to a logic 1 of the function evaluation, as shown in Figure 3a.

As shown in Figure 3c, the light (λ) from a laser source (or from the output of the previous optical network) is streamed from the BDD top node to the 1-terminal, where a photo-detector (PD) (or optical amplifier to the next computation stage) is located. The synthesis replaces each BDD node by an optical switch (S), some with a terminator at one output (ST), each controlled by an electrical primary input. Waveguides and combiners are used to connect the crossbars. When there are multiple inputs to a crossbar, optical combiners (CB) are used to merge the inputs. From this configuration, we can see that the output of the optical network is a logical 1, if the PD can detect some light at the 1-terminal, otherwise it is a logical 0.

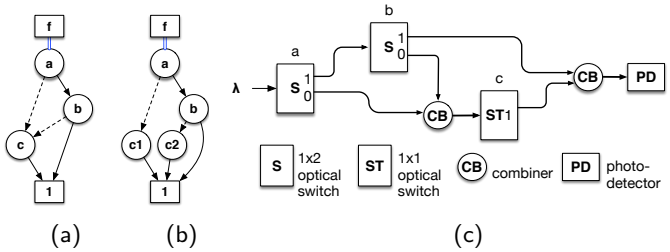

Figure 3: (a) 1-terminal BDD (b) Combiner elimination (c) BDD-based synthesis [11].

The limitation of both synthesis works [11, 22] is that they contain a great number of optical splitters or combiners, each resulting in a 3dB optical power loss, and the loss cascaded inevitably leads to an extremely weak output signal indistinguishable from noises. [12] proposes to mitigate the issue significantly using two techniques: coupler assignment and combiner elimination.

For example, the implementation in Figure 3c simply uses Y-branch combiners to connect the optical components, which always half the incoming optical powers. However, if we can leverage directional coupler discussed in Section 2, with a careful assignment of the coupling ratio, the optical power can be better exploited. As an example, in the implementation in Figure 3c, assuming zero loss on the switches, the worst-case ratio of the output optical power to the input power of all the three paths is 1/4 (path $a \rightarrow c \rightarrow 1$ or $a \rightarrow b \rightarrow c \rightarrow 1$). If we replace the terminal Y-branch combiner with a directional coupler with a coupling efficiency of 2/3 for port $c \rightarrow 1$ and 1/3 for port $b \rightarrow 1$, then the worst-case power ratio can be calculated to be 1/3, with an improvement of 33%. The problem is essentially a constrained polynomial programming problem, where the objective is to maximize the worst-case output optical power, the variables are the coupling ratio of each directional coupler, and the constraints are based on the law of conservation of energy of the couplers. However, there is no scalable solver that can solve the problem efficiently with a good quality. [12] introduces

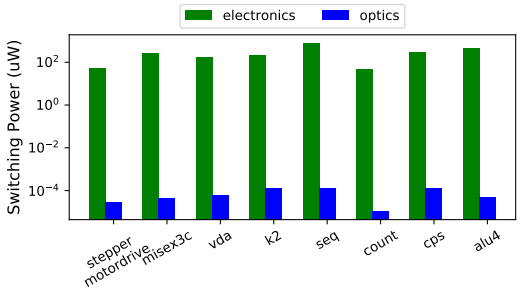

Figure 4: Switching power consumption of electronic implementation and optical implementation.

heuristics that can tackle with large-scale circuit more efficiently. Combiner elimination is another technique to improve the worst-case power efficiency. Considering the example once again, we can see if we duplicate node c and obtain the equivalent BDD in Figure 3b, the combiner at the original node c is eliminated. This also improves the worst-case power efficiency to 1/3 from the original implementation.

Figure 4 compares the switching power consumption of several benchmark circuits [24, 25] using electronics and optics. The electrical implementation was synthesized in the `gsc145nm` library under a clock rate of 1GHz. The optical implementation is based on the synthesis method of [12] using microring resonators as switches. As can be seen, the power consumption of the optics is several-magnitude smaller. The power spent in aligning the microrings is not considered here, as in more advanced optical technology the alignment would be achieved in manufacturing.

Issues and Challenges: As the circuit becomes more complex, the optical loss will become an inevitable obstacle. Hence, an interesting direction for the electronic designers would be to design novel computing schemes that leverage the strengths of optics, rather than following the CMOS logic. As an example, a recent work [26] shows that a silicon microring controlled by two electrical signals in 65nm CMOS. It can be deduced from the transmission spectra in Figure 2b that this device alone is able to implement XOR operations and save the number of optical devices. It would thus be interesting to design logic synthesis methodology with a focus on XOR logic decomposition.

Furthermore, it is also important to combine the expertise of both the optical engineers and electronic designers to find optical devices targeting at computing. For example, even though high-speed optical modulators (>50 Gbit/s) can be used in computing but their low extinction ratio jeopardizes the quality of the signal when the functionality becomes complex. However, logic computing has a greater concern in the signal quality while a lower speed (∼10 Gbit/s) would be sufficient. The reader can also refer to [27], which summarizes many other issues for optical logic computation.

3.2 Linear Optics-Based Computation

In this section, linear optics-based computation is discussed as a representative paradigm of analog optical computing. Compared with the generic computation of boolean values discussed earlier, linear optics-based computation is more functional specific but the implementation will be more compact. The paper [28] first introduced the concept of a circuit that can perform an arbitrary $N \times N$ unitary linear transformation, and based on this, [29] further adds local feedback control mechanisms. A more recent paper [30] fabricated a chip of a 4×4 universal linear optical circuit on silicon. Based on this, most recently, an ultra-fast low-power neural network has been realized [13] and has reignited the interest of optical computing.

In these works, optical matrix multiplication is commonly implemented with MZIs. In Figure 1a, one could design the MZI with two independent phase shifters, one inside the MZI ($\Delta\phi$), to induce the complementary amplitude modulation and a second at one of the outputs, which directly controls the phase ($\Delta\theta$) in the outputs. We can implement a generic 2×2 unitary ($U(2)$) operation as

$$\begin{pmatrix} a' \\ b' \end{pmatrix} = \begin{pmatrix} e^{i\theta} sin\phi & e^{i\theta} cos\phi \\ cos\phi & -sin\phi \end{pmatrix} \begin{pmatrix} a \\ b \end{pmatrix}.$$

It is proved in [28] that, by connecting multiple $U(2)$ operations into a triangle array, we can realize an arbitrary $N \times N$ unitary matrix multiplications by connecting the $U(2)$ unit. For example, [30] shows the architecture implementing a 4×4 generic matrix is realized by nine $U(2)$ units, each implementing a unitary $U(2)$ operation.

A recent application of the linear optics is a deep learning neural network demonstrated in [13], which realized a computing speed of 100 GHz and the power efficiency for forward propagation of five orders of magnitude better than conventional GPUs. In a general neural network schematic shown in Figure 5a, each node is a neuron that performs a function of $y_j = f(\sum_i (w_i x_i) + b_j)$, where each x_i is an input to the neuron, scaled by a weight w_i then the sum is shifted by a bias of b; f is a non-linear activation function. The layer transfer relation is then

$$\begin{pmatrix} y_1 \\ y_2 \\ \vdots \\ y_m \end{pmatrix} = f\Big(\begin{pmatrix} w_{1,1} & w_{1,2} & \cdots & w_{1,n} \\ w_{2,1} & w_{2,2} & \cdots & w_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ w_{m,1} & w_{m,2} & \cdots & w_{m,n} \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{pmatrix} + \begin{pmatrix} b_1 \\ b_2 \\ \vdots \\ b_m \end{pmatrix} \Big),$$

where $w_{i,j}$ is the weight of the j-th input to the i-th output of the layer. To realize this real-valued matrix in optics, singular value decomposition is used to decompose this matrix as $U\Sigma V^*$, where U is an $m \times m$ unitary matrix; Σ is a $m \times n$ diagonal matrix whose diagonal values are non-negative real numbers; V^* is a $n \times n$ unitary matrix. As discussed above, the realization of the unitary transformations U, V^* can be implemented with MZIs. The diagonal matrix Σ simply performs a *scale* operation, which can be implemented using optical attenuators or optical amplification materials. As for commonly-used activation functions as $ReLU$, $sigmoid$, $tanh$, or $Maxout$, there is no mature optical devices that can strictly perform these functions. [13] uses a simulation-based saturable absorber in the implementation. The optical implementation of the layer is shown in Figure 5b.

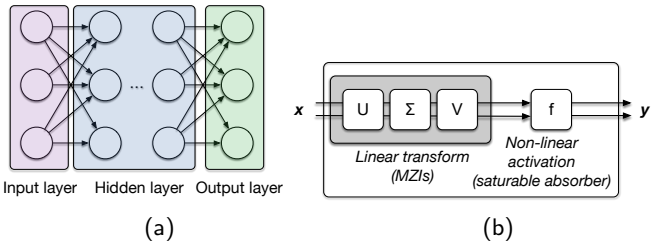

Figure 5: (a) A general neural network (b) Optical implementation of a layer.

Issues and Challenges: This pioneering work in optical neural networks also opens up a lot of research opportunities. First, the learning rate and quality of using the saturable absorber non-linearity remains a question. It

would be beneficial if the future research can investigate and find better activation functions which can be realized by optics. It would be even better, if the designer of future optical neural networks could consider the optical devices, network setup (e.g., activation function), and the architecture (e.g., including the interconnect) as a whole to fully exploit the strength of optics.

Besides forward computation, on-chip learning is also theoretically obtainable by introducing a feedback controller to each neuron. As shown in [30], a software feedback control is designed such that the circuit can adapt itself to internal signals as well as external conditions. But one problem for this controller is the introduction of optical-electrical (OE) conversion, which inevitably induces non-trivial latency and power consumption, compared with forward computation alone.

4. CONCLUSION

In this work, we survey some recent research efforts on optical computing based on SOI-based PIC, with a focus on matrix multiplication and logic functions. We also discuss the challenges and limitations of each computing paradigm. There are still many challenges and research opportunities before optical computing becomes a mainstream, for example, new optical devices, computing schemes, architectures and design automation techniques.

Scalability: The optical power loss is a major obstacle to build complex circuits. A very relevant issue to scalability is cascadability, especially in logic computation. Up to now, as optical switches lack the capability of logic-level restoration and input-output isolation as CMOS transistors, the cascadability is very limited. On-chip optical amplifiers may provide a workaround to both problems, but they also come with the overhead of area and power.

Signal integrity: The power loss is also a key reason for low signal-to-noise ratio (SNR). Furthermore, as the integration advances, crosstalk noise may also become a critical problem of the signal integrity. The crosstalk noise has already been revealed in large-dimensional optical routers [31] and it would be worthwhile to revisit the solutions in the new context of computing.

Optical memory: Optics is able to realize linear transformations and combinational functions but in order to build more practical applications, optical memory would be very desirable. [32] shows an ultra-small, low-power flip-flop memory on a silicon chip driven by light, but without a careful redesign of the overall architecture, how this device can be leveraged remains to be a question.

Robustness: Like many emerging technologies, computing optics may suffer from manufacturing defects and process/environmental variations. Robust and fault-tolerant designs that can endure these uncertainties are critical to bringing optical computing in practice.

Optical Interconnect: Optical interconnects have been intensively investigated and shown the advantage over metal interconnects in inter-chip communications [33–35]. However, the conversion between electronic and optical signals at the interconnect interface consumes a nontrivial amount of power (∼0.5pJ/bit). The power can be reduced if part of the core computing is also implemented in photonics rather than electronics. This further motivates the research of optical computing together as optical interconnect in a system.

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