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Silicon-Based Group-IV O-E-O Devices for Gain, Logic, and Wavelength Conversion

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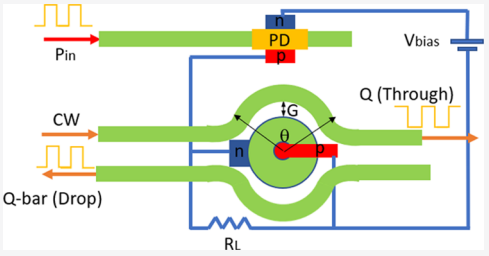
ABSTRACT: Using the strip-guided "manufacturable" SOI/GeSn group-IV integrated-photonics platform operating at 1550 nm, we propose an optical-to-electrical-to-optical (O-E-O) device that can work either as an amplifierless optical repeater with gain, as a linear-optics wavelength-converter repeater, or as a new "optical−optical" logic (OOL) gate. An interconnected array of such linear-optics gates performs complicated digital-logic functions. The OEO comprises a photodetector (PD), an electro-optical modulator (EOM), and an electrical biasing-and-interconnect circuit. A digitally modulated optical signal is sent into a waveguided photoconductive GeSn PIN PD whose electrical output is compatible with the electrical input of a resonant bus-coupled Si PN-depletion microdisk EOM modulating a CW optical input beam. Our self-consistent physical model takes into account N and P doping effects. Assuming a peak optical input power of 0.5 mW and 3 V DC bias, our 1.55 μm simulations predict successful repeater-converter operation at 6.5 GHz (13 Gbit/s) and successful OOL functioning at 4.7 GHz (9.4 Gbit/s), with 12-to-16 dB extinction ratio and switching energy in the 5.8 to 9.6 fJ/bit range. A further increase of the OOL bit rate to 14 Gbit/s is available at the expense of an increased optical signal power.



KEYWORDS: *Group IV photonics, Electro-optical modulator, Logic gates, Microdisk, Optical computing*

This theoretical paper proposes and analyzes a "multi-function" optical-to-electrical-to-optical (O-E-O) device based on the group IV technological platform. The device has two optical inputs and one optical output. A modulated optical input "A" is sent into a photodetector (PD), while at the same time a CW light beam is sent into an electro-optical modulator (EOM). An electrical circuit that includes DC bias connects the PD's electrical output to the EOM's electrical input. Thereby, the modulated CW beam (the output beam) reproduces faithfully the modulation on "A". By selecting a CW optical power that is larger than that of "A", the output peak level exceeds the input peak level, providing optical gain; in other words, the modulated input is regenerated and is restored at a higher level.

The present device is similar in many ways to the device presented by Nozaki et al.;[1] however, here we have made significant changes, improvements, and functional expansions to the Nozaki device, as follows: (i) we adopted the SOI/GeSn group-IV integrated-photonics platform that is arguably more amenable to low-cost high-volume manufacture than is the InP/InGaAsP platform; (ii) we operate at the 1550 nm telecom wavelength, although the proposed device is suitable to operate at the "new" 2000 nm optical communications wavelength;[2] (iii) our device uses strip-channel waveguides and a bus-coupled microdisk resonator-waveguide rather than the 2D photonic-crystal embodiment[1] of line-defect waveguides and point-defect resonators (these strips offer larger-scale photonic integration than 2D PhC circuits because the PhC slab suffers from propagation losses); (iv) compatibility of the PD O-E conversion with the EOM E-O conversion is obtained by choosing a reverse-biased GeSn PIN PD operating in the photoconductive mode to work with a Si vertical-junction PN disk operating in its carrier-depletion mode; (v) monolithic integration of PD and EOM is proposed, rather than the hybrid InGaAsP integration of Nozaki.

Our device works as an amplifierless optical repeater and/or as a wavelength converter offering up-conversion or down-conversion, with the selected conversion wavelength being anywhere from 1200 to 2500 nm. The optical input is spectrally broadband due to the PD's property. We have proposed a new OEO function for our device which is optical−optical logic (OOL) gating that is enabled by adding a second modulated optical input B to the existing A input and by coupling a second strip bus waveguide to the EOM in order to attain a complementary logic-modulated output (Q-bar) in

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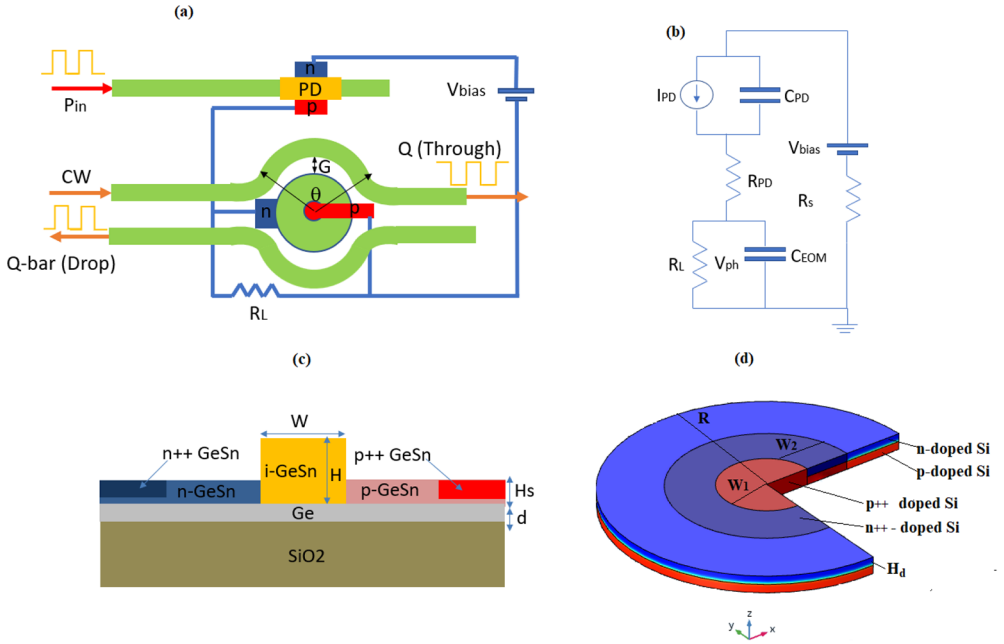

Figure 1. (a) Schematic top view of proposed optical-to-electrical-to-optical device; (b) Equivalent electrical circuit of O-E-O; (c) Photodetector cross section; (d) Disk modulator architecture (cover is SiO_2, not sketched for reasons of clarity).

addition to the original output (Q). It is a linear-optics solution rather than a nonlinear optical technique.[3−5]

As detailed below in this paper, the DC bias voltage supplied within the electrical circuit that joins PD to EOM assures that the EOM will remain reverse-biased for large values of the A-input powers, powers that are needed to supply a large-enough AC voltage at the EOM. This type of EOM has a successful history in high-speed, energy-efficient optical modulation[6] as well as in "electro optical logic".[7]

The results given below predict OEO structures with very low capacitance and ultralow driving energy. However, our analysis finds two restrictions imposed upon the OEO structures. First, the wavelength of the CW source must be matched closely to the V = 0 resonance wavelength of the EOM. Second, the high-quality-factor EOM that is used here has an equivalent capacitance ranging between 5 and 6 fF, which restrict its digital modulation rate to 6.5 and 4.7 GHz for repeater and OOL applications, respectively. The CW source can be an on-chip laser diode (hybrid or monolithic) or an external laser coupled to the chip. The sections of this paper, given below, describe the OE and EO property optimization of the electrical biasing-and-interconnect circuit, the optimized disk designs, and the optical−optical logic gate (OOL) architectures.

PROPOSED OEO DEVICE AND NUMERICAL RESULTS

Figure 1a shows the proposed device structure and its operation scheme. An input optical signal with a peak power of P_{in} and a wavelength of λ is injected into the PD. The generated photocurrent (I_{pd}) induces a photovoltage (V_{ph}) across the load resistance (R_L), as given by $V_{ph} = \eta_{pd}P_{in}R_L$, where η_{pd} is the photodetector responsivity operating in the photoconductive mode.

In this context, as V_{ph} increases from V_{ph}= 0, the resonant spectrum of the disk EOM is red-shifted as a result of the carrier depletion effect. In Figure 1b, the equivalent circuit of O-E-O device is shown. Here I_{pd} and V_{ph} are considered "AC", while V_{bias} is DC. In our investigations, the PIN PD is a p-GeSn/i-GeSn/n-GeSn homojunction[8] photodiode embedded in a waveguide as shown in Figure 1c. The GeSn waveguide is a ridge structure having height H, width W, and slab thickness H_s. The ion implantation is performed at both lateral ends of the slab in order to fabricate the p and n regions as well as the p++ and n++ contacts. Moreover, a Ge layer with a thickness d is included in order to facilitate the deposition of the GeSn alloy. Although a Ge-on-Si PD device certainly absorbs 1550 nm photons, we think that the Ge choice is not optimum and that a GeSn layer gives superior results. Compared with present Ge-on-Si PDs, the GeSn-on-Si PD gives better wavelength coverage due to its selectable bandgap. Most importantly, the 1550 nm GeSn-on-Si PD has stronger absorbance (15 000 cm^{-1}), higher efficiency, and lower spatial volume. Another potential advantage of our approach is that hundreds or thousands of PDs could be closely integrated on-chip at a low cost of production. In our approach, the Sn content of the GeSn layer is tailored to the wavelength of operation to give optimized absorption, namely 3% concentration for 1550 nm and 10% for 2000 nm.[9] As a result, our proposed OEO device is suitable for operation at 2000 nm, representing a "new frontier" for group IV integrated photonics.[2] There are reasons to believe that the GeSn-PD fabrication is quite compatible with present-day silicon photonics fabrication. Regarding the related GeSn epitaxy needed here, the GeSn chemical-vapor deposition has two chemical precursors rather than the single precursor employed for elemental Ge CVD. Successful experiments on bufferless growth of GeSn on Si made use of the germane and stannane precursors.[10] So, the GeSn CVD is arguably not very different from the Ge germane CVD. Also, recent developments within electronics foundries have shown that GeSn is successfully incorporated as a transistor source and drain.

Looking at Figure 1a, we propose fabrication of a strip-etched SOI waveguide structure for the channels as shown in

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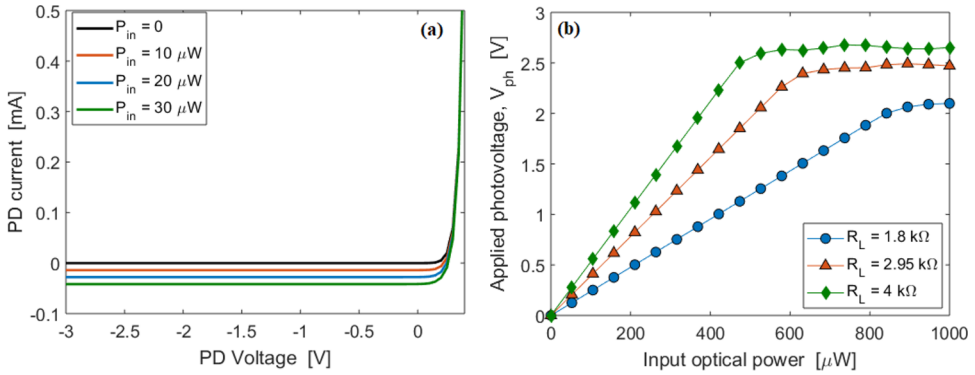

Figure 2. (a) PD current as a function of PD voltage for different values of the input optical power. (b) Photovoltage across the load resistance as a function of the input optical power, for different values of R_L, assuming bias voltage V_{bias} = 3 V DC.

green. After that, a trench would be etched down to the buried oxide at the end of the input strip waveguide, and in that trench selective-area epitaxy of Ge would be performed to provide an ultrathin Ge virtual substrate for the PD. Next, the epitaxy of the GeSn film in the same small area would be carried out, followed by ridge-etching of GeSn and laterally located doping of GeSn. In our O-E-O device, the EOM is a vertical-junction disk operating in the carrier-depletion mode (a viable alternative to this depleter, possibly superior, is the Franz–Keldysh E-field PIN disk modulator that shall be the topic of a future study). Moreover, we guess that our architecture is suitable to be implemented in an EOM based on the SiGe platform.[11] Figure 1d shows the architecture of the EOM used in the present analysis, together with its fundamental geometrical and physical parameters.

A second output bus waveguide is shown in Figure 1a so that we can obtain the detailed performance required for the OOL application. Moreover, the architecture of Figure 1a shows the geometrical parameters of the curved, constant-gap directional coupler (DC) between disk and bus waveguide where the transition between the straight and the curved sections in the bus waveguides can be fabricated by using an S-shaped profile. Examining first the PD response, a detailed analysis of absorption coefficient and refractive index for $Ge_{1-x}Sn_x$ alloys is presented in ref 12, where it is demonstrated that an absorption coefficient as large as α = 15 000 cm^{-1} can be obtained by setting $x \sim 3\%$ and ~10% for λ = 1550 and 2000 nm, respectively. Hereinafter, we analyze the PD performance assuming the $Ge_{1-x}Sn_x$ region with α = 15000 cm^{-1}.

We begin with simulation of the O-E-O device operating at 1550 nm. In this context, we take the input SOI waveguide to be a standard strip waveguide having height H_{SOI} = 220 nm and an initial width W_{SOI} = 400 nm, tapered to W_{SOI} = 500 nm in order to improve the end-fire coupling to the PD waveguide. Moreover, the PD efficiency is strongly dependent on the product $\eta_{coup} \times \eta_{abs}$, where η_{coup} is the efficiency for the end-fire coupling, η_{abs} is the absorption efficiency inside the absorber $Ge_{0.97}Sn_{0.03}$ layer. The contribution η_{coup} depends strictly on the SOI and PD waveguide cross-section. In this context, simulations performed by means of a commercial software based on full-vectorial FEM,[13] indicate that η_{coup} is around 94.6% by fixing $W = W_{SOI}$, $H = H_{SOI}$, H_s = 100 nm, and d = 50 nm. In addition, the term η_{abs} is calculated by $\eta_{abs} = 1 - e^{-\gamma\alpha L}$ where γ and L are the optical confinement factor inside the $Ge_{0.97}Sn_{0.03}$ layer and PD length, respectively. In our device, η_{abs} ranges from 99% and 100%, when changing L from 5 to 10 μm, respectively. In this context, the PD behavior under illumination is determined as a function of the optical generation rate, G_{op} [m^{-3} s^{-1}], evaluated by applying eq 1:

$$G_{op}(\omega) = \frac{-0.5\,\mathrm{real}(\mathrm{div}(\mathbf{S}))}{\hbar\omega} \quad (1)$$

where **S** is the Poynting vector of the optical mode propagating inside the PD waveguide.

The following analysis is based on the FEM multiphysics approach as described in the Numerical Simulation Method section. Current–voltage FEM simulations are performed for different values of the input optical power P_{in} (inside the SOI waveguide) ranging from 0 to 30 μW and are plotted in Figure 2a, reflecting the characteristic of a p–i–n diode. The obtained data lead to an estimated responsivity η_{pd} = 1.4 A/W in the photoconductive mode. The photocurrent of the simulated PD is extremely linear with respect to the input light level. Generally speaking, the lower limit of this linearity is determined by the noise equivalent power (NEP), while the upper limit is strongly dependent on the electrical circuit connected to the PD. In this sense, Figure 2b shows the photovoltage V_{ph} as a function of the input optical power, for different values of the load resistance (R_L), assuming the reverse bias voltage V_{bias} = 3 V DC. Moreover, in the simulations, we have assumed the serial resistance of the PD (R_{PD}) and the external termination resistance (R_s) as 1 kΩ, and 50 Ω, respectively.

The plot shows clearly the upper limit of linearity. In particular, the P_{in} saturation limit and the slope of the photovoltage response increase when the load resistance is increased. Figure 2b shows that the single GeSn p–i–n PD generates an "AC" photovoltage of over 2.65 V without using any electric amplifier. This demonstrates the possibility of adopting our group IV O-E-O device for realization of amplifier-free OOL gates (see the following section).

At this stage, having determined the photovoltage, we characterize EOM disk behavior. In the EOM, we require a large wavelength shift per AC volt ($\eta_\lambda = \mathrm{d}(\Delta\lambda)/\mathrm{d}V$), and a high-quality factor Q_f so that a "low" photovoltage induces a resonance shift equal to the disk's line width. However, we find that these requirements are conflicting. With reference to the disk architecture shown in Figure 1d, we assume W_1 = 600 nm, W_2 = 600 nm, H_d = 220 nm, and R = 2 μm. The doping regions in this disk introduce large concentrations of free holes and electrons overlapping with the whispering-gallery mode (WGM), resulting in a reduction of the refractive index and an

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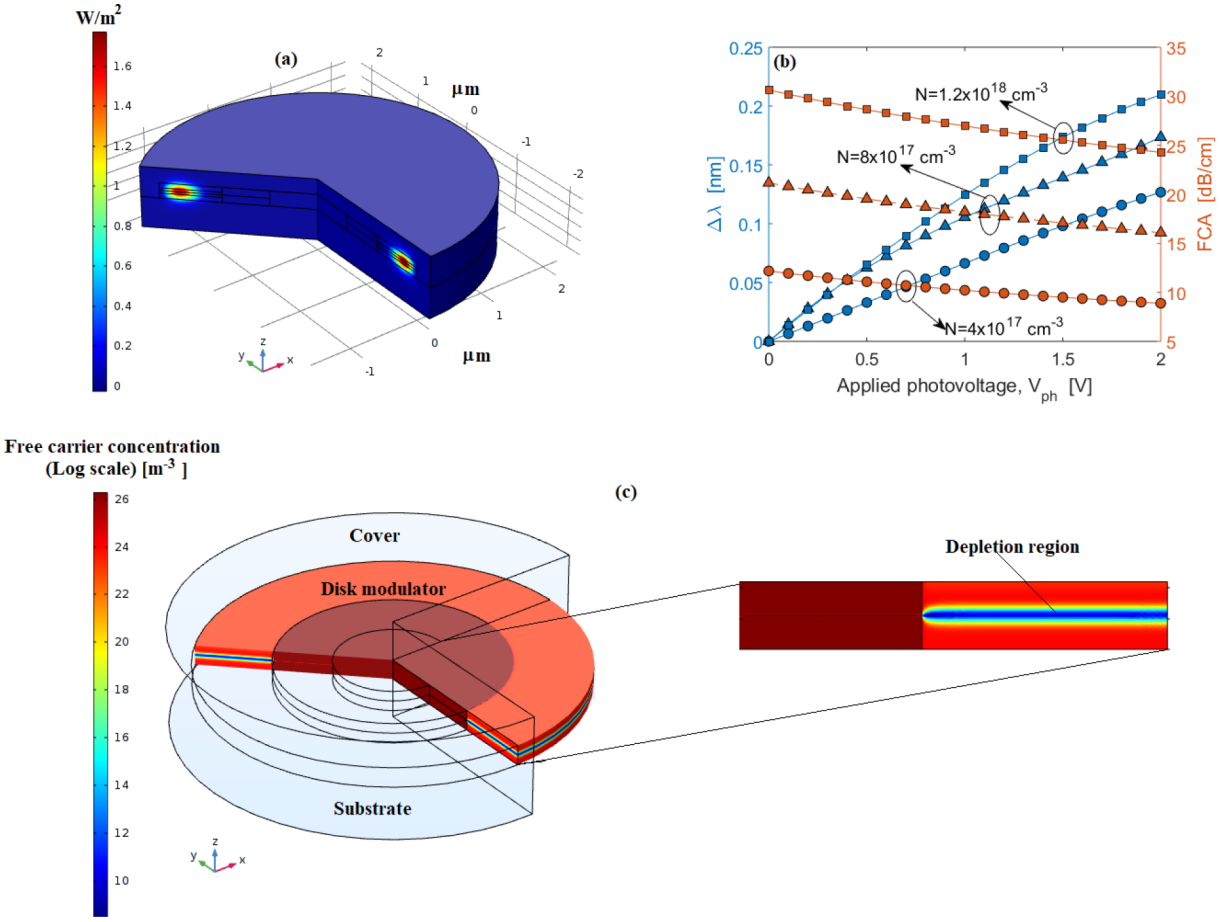

Figure 3. (a) Poynting vector of the WGM propagating inside the disk; (b) Differential resonance wavelength shift and differential disk line width as a function of dopant concentrations; (c) Free carrier concentration (log scale) distribution inside the disk.

increase of absorption losses. This is clearly evident in Figure 3a where the spatial distribution of the Poynting vector for the fundamental WGM is shown, assuming that the EOM disk is not biased (rest condition). When a reverse bias is applied to the vertical PN junction, an increase in its depletion width is induced.

As a result, the WGM overlaps with fewer free carriers, increasing the WGM's effective refractive index and redshifting its transmission spectrum while at the same time decreasing the infrared absorption and reducing the resonance line width. The effect of large dopant concentrations is to induce a small depletion width at the rest condition (H_{depl}), causing the overlap between the depletion region and the WGM to be mainly focused in the center of the mode distribution. As a result, larger wavelength shifts per volt ($\eta_\lambda = d(\Delta\lambda)/dV$) and larger free carrier absorption (FCA) are promoted because the increase of depletion width with reverse voltage overlaps again mainly the center of the mode distribution.

The opposite trend is recorded in the case of low doping. Indeed, although in the unbiased condition the larger H_{depl} induces larger overlap with the optical mode, η_λ becomes smaller since a further increase of the depletion region tends to overlap with the WGM tails. In order to determine the design rules, we assume the junction target p-type and n-type doping concentrations as a parameter. In this context, the n-doped region extends to the outer edge of the disk, and it has a concentration N_d [cm^{-3}] (assumed as a design parameter) and a depth of 0.11 μm. Likewise, the p-doped region underneath has a concentration N_a [cm^{-3}] (assumed as a design parameter) and a height of 0.11 μm. Underneath the grounded metal contact and active metal contact is a highly doped p+ region and n+ region, respectively, with a concentration of 3×10^{20} cm^{-3} (see Figure 1c). The results of the multiphysics approach are summarized in Figure 3b, where the resonance shift $\Delta\lambda$ and the FCA coefficient are plotted as a function of the applied photovoltage (V_{ph}), for different dopant concentrations ($N_d \sim N_a \sim N$). The simulation results show the trend discussed above. The plot indicates that, at V_{ph} = 1 V, $\Delta\lambda$ ranges from 0.066 to 0.135 nm when changing N from 4×10^{17} to1.2×10^{18} cm^{-3}. For the same conditions, the FCA coefficient changes from 10.2 to 27.0 dB/cm. This result is comparable to the resonance shift of similar devices with standard dopant concentrations.[6,7,14] Assuming this implantation profile (see Numerical Simulation Method section), the FEM simulation is presented in Figure 3c, where the free carrier concentration (log scale) is plotted inside the disk modulator for a photovoltage value of 1 V. The plot clearly shows the graded depletion region. We note that a further optimization could be obtained by shifting the junction slightly toward the n-doped region. As a result, greater overlap of the optical mode with holes is obtained, providing a larger change in the real part of the refractive index and a smaller change in the imaginary part relative to electrons.[16,17] However, according to eq 3, a reduction of the disk line width induces a reduction of the optical modulation bandwidth. Thus, a

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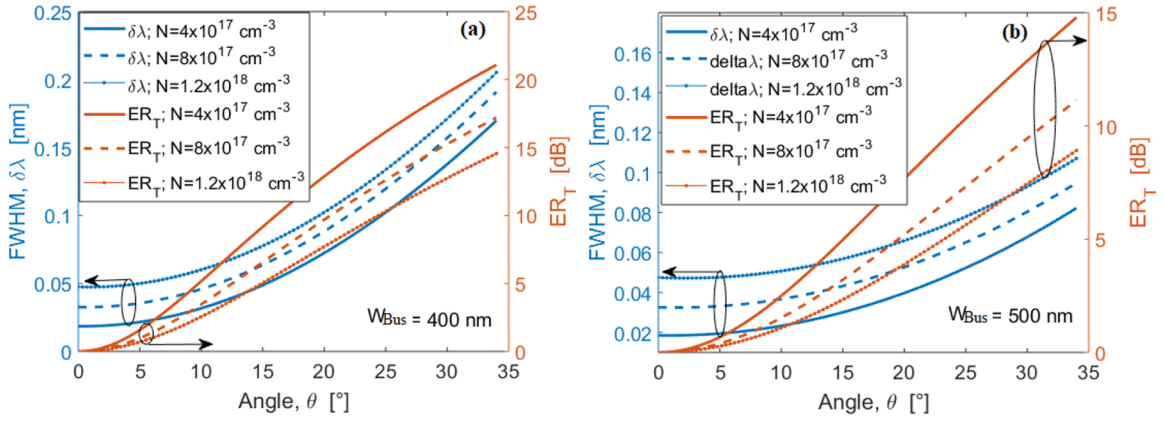

Figure 4. (a) Disk line width and extinction ratio at the Through port as a function of the coupler angle, for W_{Bus} = 400 nm; (b) Disk line width and extinction ratio at the Through port as a function of the coupler angle, for W_{Bus} = 500 nm.

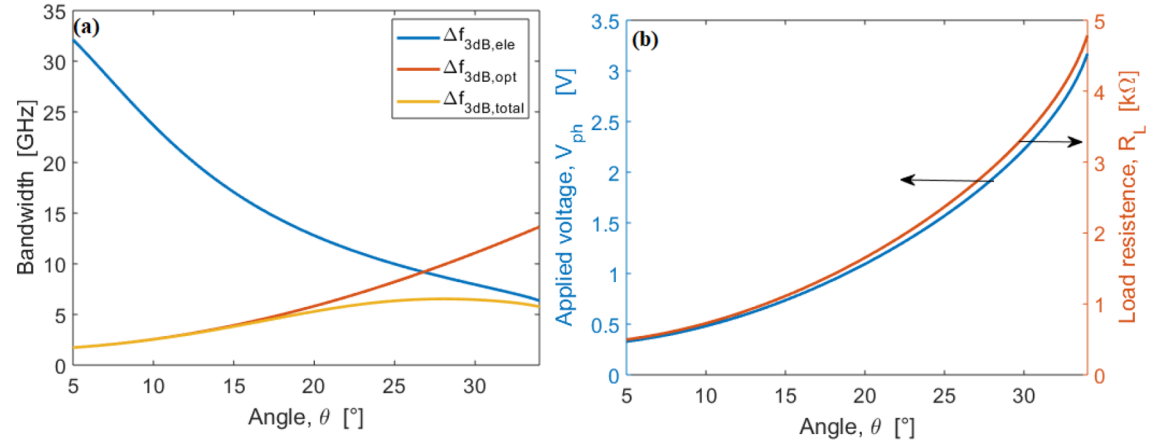

Figure 5. (a) OEO bandwidths as a function of the coupler angle under the condition $\Delta\lambda = \delta\lambda$; (b) Applied photovoltage and load resistance as a function of the coupler angle, satisfying the condition $\Delta\lambda = \delta\lambda$.

trade-off between conflicting requirements is proposed in the present analysis.

Although any shape and architecture of the directional coupler (DC) between EOM disk and bus waveguides can be practically designed and fabricated, a pulley DC with gap G and coupler angle θ, has been employed in the following investigation, as sketched in Figure 1a, where the transition between straight and curve sections in the bus waveguides can be fabricated by using a S-shape profile. In general, the pulley coupling provides more degrees of freedom in the design particularly when a strong asynchronism between the disk modulator and the bus waveguide occurs.[15,18] Following the method proposed in ref 18, Figure 4a,b show both the disk line width ($\delta\lambda$) and the extinction ratio at the Through port (ER_T) as a function of the coupler angle θ for various dopant concentrations ($N_d \sim N_a \sim N$) and bus waveguide width (W_{Bus}) of 400 and 500 nm, respectively. In the simulation, the gap G between the EOM disk and the bus waveguides is assumed to be 100 nm. The plots indicate that for a given value of angle θ, both the ER_T and $\delta\lambda$ increase with the doping concentration. For example, setting θ = 25°, the simulations record ER_T from 16.2 dB (10.4 dB) to 10.4 (5.7 dB) when changing N from 4×10^{17} to 1.2×10^{18} cm^{-3} and for W_{Bus} = 400 nm (500 nm). In the same conditions, the line width $\delta\lambda$ ranges from 0.10 nm (0.052 nm) to 0.134 nm (0.078 nm). Thus, with the aim of realizing an OEO device having a large ER_T, we assume $N = 4 \times 10^{17}$ cm^{-3} and W_{Bus} = 400 nm as a good trade-off. Moreover, the design value of the coupler angle is determined in order to maximize the device bandwidth. A direct application of the OEO device as sketched in Figure 1a is the digital optical repeater. In this context, the logic level "1" of a digitally modulated optical input beam should produce a photovoltage value able to cause a shift of the resonance spectrum of about 100% of the 3-dB resonance line width. In the following, we analyze the bandwidth features under this 100% rule. The total 3-dB bandwidth ($\Delta f_{3\,dB,tot}$) of the OEO device can be estimated by means of eq 2:

$$\Delta f_{3dB,tot} = \frac{\Delta f_{3dB,ele} \times \Delta f_{3dB,opt}}{\sqrt{(\Delta f_{3dB,ele})^2 + (\Delta f_{3dB,opt})^2}} \quad (2)$$

where $\Delta f_{3\,dB,opt}$ represents the optical modulation bandwidth given by[6]

$$\Delta f_{3dB,opt} = \sqrt{\sqrt{2} - 1}\,\frac{c_0 \times \delta\lambda}{\lambda_0^2} \quad (3)$$

where c_0 and λ_0 are the vacuum light velocity and the disk resonance wavelength, respectively. The term $\Delta f_{3\,dB,ele}$ is the RC bandwidth, calculated from the equivalent circuit of Figure 1b.

Our FEM simulations indicate that the capacitance related to the photodetector (C_{PD} see Figure 1b) is estimated as about

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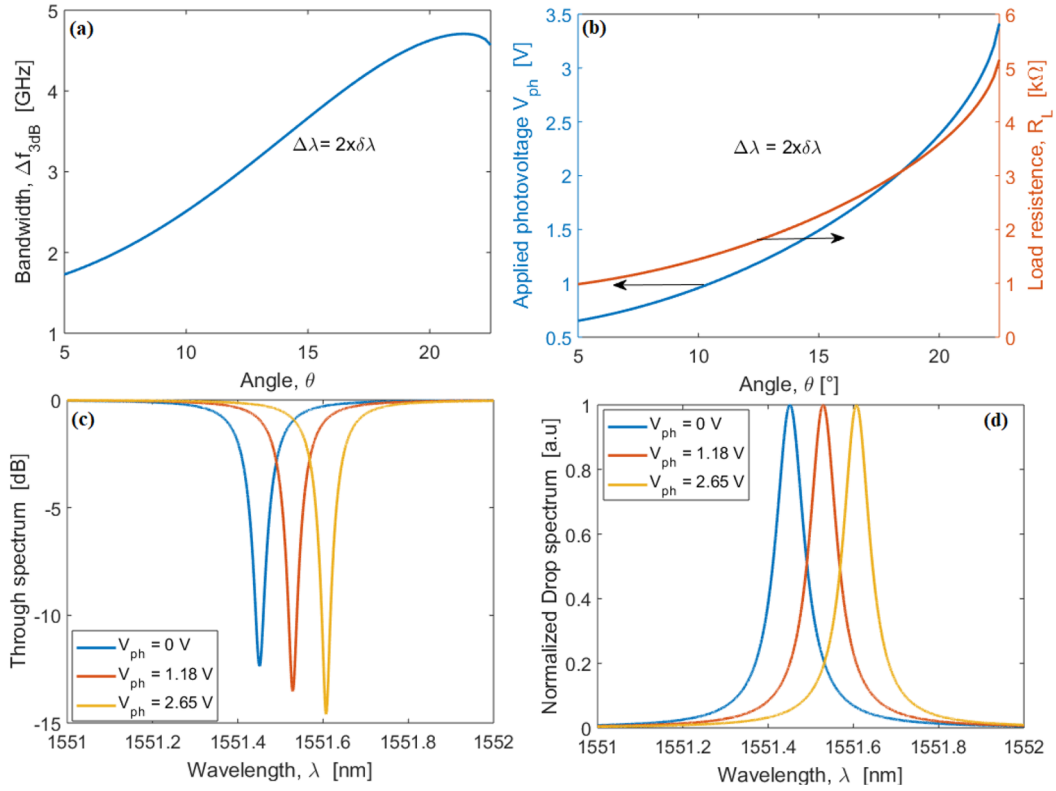

Figure 6. (a) OEO total bandwidth as a function of the coupler angle under the condition $\Delta\lambda = 2 \times \delta\lambda$; (b) Applied photovoltage and load resistance as a function of the coupler angle, satisfying the condition $\Delta\lambda = 2 \times \delta\lambda$; (c) Through spectrum, for different values of the applied photovoltage; (d) Normalized Drop spectrum, for different values of the applied photovoltage.

0.36 fF. In this context, Figure 5a shows the electrical, photonic, and total bandwidths as a function of the coupler angle under the condition $\Delta\lambda = \delta\lambda$ and assuming P_{in} = 0.5 mW. The plot indicates that for $\theta < 28°$, the OEO device is dominated by the photon lifetime, $\tau_{ph} = \lambda_0^2/\pi c_0 \delta\lambda$, while it is RC limited for $\theta > 28°$. Figure 5b plots the applied photovoltage and the load resistance needed to induce the condition as a function of the coupler angle. The curves reveal that both the applied photovoltage and the load resistance needed to induce the condition $\Delta\lambda = \delta\lambda$, increase with an increase in the coupler angle. However, for θ = 28°, we find the maximum total bandwidth (BW) evaluated as 6.53 GHz, corresponding to a bit rate = 2 × BW = 13 Gbit/s, a disk modulator capacitance C_{EOM} = 6.14 fF, V_{ph} = 1.95 V and R_L = 2.95 kΩ. Under this condition, we record the insertion loss at the Drop port of about 1.4 dB (no Bias), ER_T = 16.6 dB (no bias), and $\delta\lambda$ = 0.12 nm. Moreover, according to ref 7, the switching energy per bit is estimated as 5.83 fJ/bit.

In the OOL scenario, we need an applied photovoltage value that is large enough to cause a resonance shift of 140-to-200% of the 3-dB resonance line width (see the following section). Under this 200% rule, Figure 6a shows the total bandwidth as a function of the coupler angle under the condition $\Delta\lambda = 2 \times \delta\lambda$ and assuming P_{in} = 0.5 mW. The plot indicates that for θ = 21° the OEO device records the maximum total bandwidth as 4.57 GHz, corresponding to a bit rate = 9.14 Gbit/s, a disk modulator capacitance C_{EOM} = 5.48 fF. Moreover, the applied photovoltage and the load resistance values needed to induce the condition $\Delta\lambda = 2 \times \delta\lambda$, are plotted in Figure 6b, i.e. V_{ph} = 2.65 V and R_L = 4 kΩ at θ = 21°. Under these conditions, we find an insertion loss at the Drop port of about 2.4 dB (no bias), ER_T = 12.3 dB (no bias), $\delta\lambda$ = 0.078 nm, and the switch energy per bit equal to 9.6 fJ/bit. Finally, the Through and normalized Drop spectra for different values of the photovoltage are plotted in Figures 6c,d. It is worth outlining that the obtained BW is the result of the trade-off between conflicting requirements such as large resonance shift per volt, small $\delta\lambda$, and low P_{in}. Our investigations record that degree of freedoms for further and substantial reduction of C_{EOM} are not possible. Thus, the only way to improve the bandwidth is to operate with larger values of P_{in}. In particular under the condition $\Delta\lambda = 2 \times \delta\lambda$ and assuming P_{in} = 1 mW, we record a BW = 6 GHz (bit rate = 12 Gbit/s). Moreover, for P_{in} > 2 mW, the total 3-dB bandwidth of the OEO device is limited exclusively by the optical modulation bandwidth, assuming a value of 6.72 GHz. According to eq 3 and operating at large value of P_{in}, a further improvement of the bandwidth could be obtained by increasing $\delta\lambda$, by changing the doping levels and the pn junction position.

THE OPTICAL COMPUTING CONTEXT

We would like to place our gain, wavelength conversion, and logic devices in the larger context of digital optical computing (DOC). Nowadays, the field of "optical computing" includes many analog neuromorphic approaches that have a bright future in computing. However, in addition to neural system progress, significant developments have been made in DOC, and we predict important DOC advances in the future. Here we will briefly sketch the past, present, and future of DOC. Using mainly bulk optics, DOC began about 50 years ago. The field faded out and then became reborn with the advent of manufacturable photonic integrated circuits whose compo-

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nents are micron-scale with an energy drive of femtoJoules per bit. Regarding optical logic devices, the electro-optical logic (EOL) devices really stemmed from theoretical and experimental work reported on "directed logic" (DL)[19,20] since the DL is a more general formulation. And now OEO and OOL are ripe for exploitation. The self-electrooptical device,[21] with its nonlinear bistable response and its two optical terminals, is fundamentally different from the OEO. Comparing EOL and OOL gates, there is a penalty for cascading EOL gates since the overall optical loss builds up with the cascade. Unlike the series connection of EOL, it is easy and advantageous to cascade many OOL gates because the cascade will be lossless. However, there is a "power requirement" on the CW light source or sources that feed this cascade. For example, if there are N gates and one source, then the source output is divided into N branches. Consequently, the cascade source must have N-times the power output of the source needed for one gate.

The modern transistorized all-Electronic Digital Computer (EDC) is the gold standard, but the new developments of EOL and OOL beg the question: What is the practical application of this logic? The answer is seen in the embodiment of a new computer, the electronic-photonic digital computer (EPDC) that uses the best of both worlds. By inserting low-latency high-performance optical logic circuits into portions of EDC, the EDC is transformed into EPDC offering higher performance metrics than those of the original computer. Examples of EPDC logic research directions are a new full adder that combines transistor gates with EOL.[22] More generally, we predict that a new and more-effective matrix multiplier can be constructed from OOL-and-transistors in combination with OEO and EOL. The EPDC logic applications can advantageously utilize the unique aspects of light such as wavelength-division multiplexing and the wavelength conversion in this paper. Another strategy for effective EPDC logic insertion is to utilize the multioperand logic described in ref 23. In cases where the logic circuit is only EOL,[24] the OEO "repeater" devices are readily inserted into the circuit to boost signals and to reduce the bit error rate.[25] To supplement the EP logic circuits, the memory portion of the EPDC can be enhanced by using photonic components to create an electronic-photonic content addressable memory.[26] In summary, the EPDC has the potential to advance DOC in a major way.

A competitive kind of computing, photonic quantum computing (PQC), is now emerging, and there is strong research momentum in this PQC field. The PQC has the potential to make large impacts. However, many challenges remain and there are two caveats. First, it will take several years of research work for the present superconducting single-photon detectors (SPDs) used in PQC to be replaced by room-temperature SPDs that ensure ubiquitous chip application. Second, the PQ computer is not a general-purpose computer, which means that the computation relies upon specialized algorithms such as Shor's algorithm.[27] PQC can accelerate certain calculations but does not truly replace the present logic-based central processor units. In other words, PQC applications do not completely overlap EPDC applications. In contrast to PQC, optical computing based on logic already has a mature platform and an extremely capable CMOS manufacturing line. Development of OOL gates and OEO, along with EOL, will give EPDC the opportunity to "go beyond" transistors and continue Moore's law in the near future.

PROPOSED OOL GATES AND ANALYSIS

This section proposes and analyzes the design of new optical−optical logic (OOL) gates that have two optical input paths and one "processed" optical output, specifically the AND, OR, NAND, NOR, XOR, and XNOR OOL gates. A single-input, single-output NOT gate is also presented.

Within the field of digital optical computing, there is extensive literature on the electro-optical logic (EOL) approach[28−34] and the "all-optical logic" or OOL approach.[5,35] The EOL suffers from an optical insertion loss penalty when several gates are cascaded, and the repertoire of possible EOL gates is somewhat limited. OOL has always been seen as a nonlinear optical (NLO) approach in which a strong optical pump works in concert with a weaker optical probe within an NLO material structure. The present OOL paper moves away entirely from the NLO approach and proposes instead a new linear-optics structure that converts coded light from the optical domain into the electrical domain (O-to-E, or OE), followed immediately by a second conversion where the electrical signal triggers an optical response (E-to-O, or EO).

The present OOL design is based to a large extent upon the paper by Nozaki et al.[1] in which a three-optical-beam device is demonstrated. Their structure had two input beams and one output beam, giving three "optical terminals." We have expanded their device to a "five terminal" device having three optical inputs and two optical outputs labeled A, B, CW and Q, Q-bar, respectively. The Nozaki structure had OE + EO, whereas ours has OE + OE + EO; that is, two simultaneous OE conversions, followed instantly by EO.

The Nozaki device utilized a planar, integrated 2D-photonic-crystal platform. When we consider the optical propagation losses within this 2D "circuit" and the difficulties of interfacing of that circuit with conventional strip waveguides, we conclude that the 2D PhC structuring is not the optimum technique. We have invented an alternative integrated-photonics method that appears to be more practical. Proposed here is a foundry-compatible platform employing one of the present popular photonic integrated circuit (PIC) technologies that uses exclusively strip waveguides. Our estimation is that this will give performance metrics for the novel OEOEEO devices that are superior to those of their 2DPhC counterparts. Specifically, the line-defect waveguides in the 2DPhC are replaced by strips channels and the photodetector (PD) material is embedded in a strip having PIN side electrodes. The points-defect electro-optical (EO) resonator in the 2D PhC can be replaced quite effectively by either: (i) a standing-wave EO nanobeam or Bragg-grating resonator within a strip or (ii) a traveling-wave EO microring or microdisk resonator side-coupled to a strip bus waveguide or to two such buses. The disk electro-optical modulator (EOM) is used here. The wavelength of light for CW input to EOM is the same as that used for the A and B logic-light inputs to the PDs. This is a special case of Nozaki's wavelength converter.

Our prediction is that when the OEOEEO structure is implemented in the factory-PIC platform, the high speeds and very low voltages and extremely low switching energies of the Nozaki approach will be preserved if not improved upon. Because CW is selected as more powerful than A, B, complete restoration of the A, B signal levels is attained at the Q and Q-bar gate outputs as in an "amplifying repeater." Optical gain is also available if desired. Because A and B are, in effect, not attenuated in the present logic application, a low-latency and

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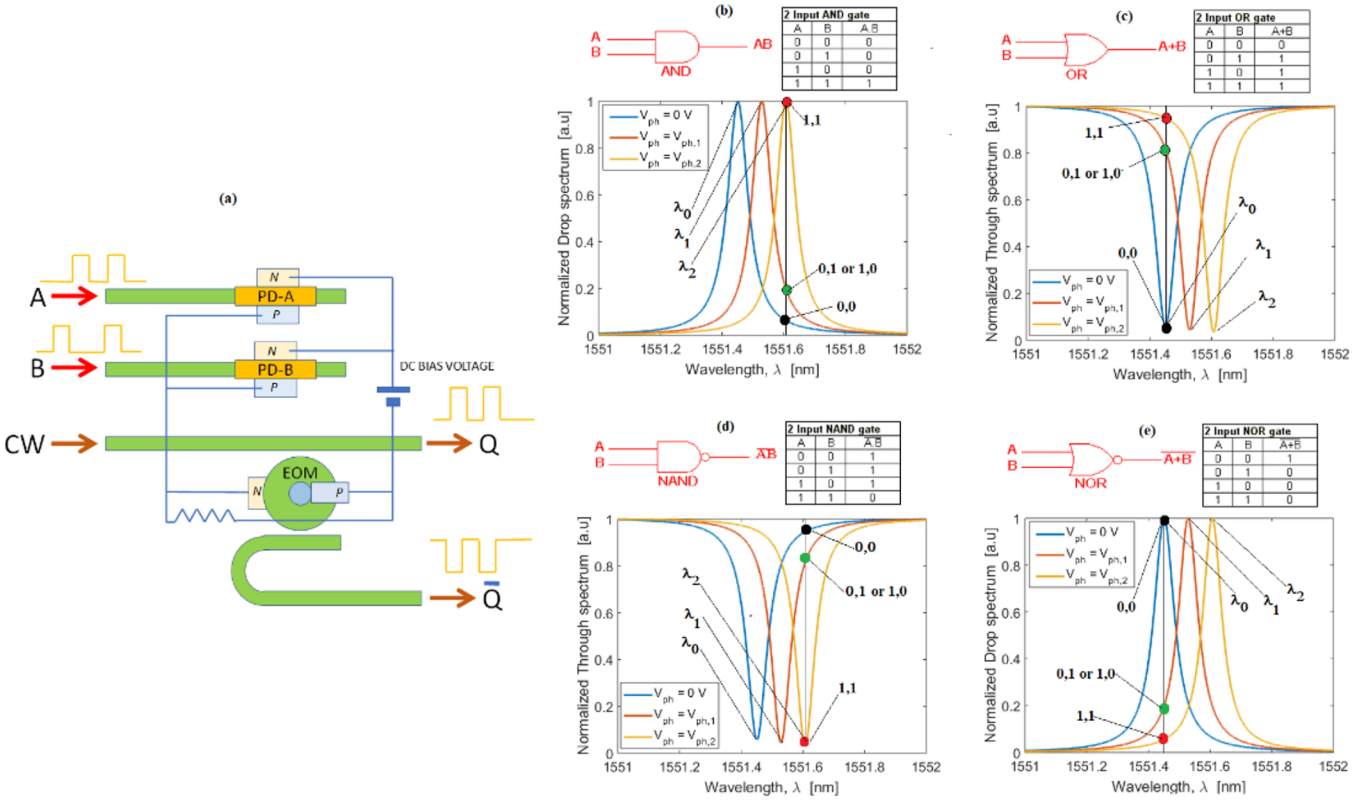

Figure 7. (a) Schematic top view of proposed optical-to-electrical and electrical-to-optical AND, OR, NAND, and NOR logic gates in a strip-waveguided photonic-integrated circuit; (b) Design of an OO AND gate, the required truth table, and the required Q-bar output and λ_2 operation; (c) Design of an OO OR gate, the required truth table, and the required Q output and λ_0 operation; (d) Design of an OO NAND gate, the required truth table, and the required Q output and λ_2 operation; (e) Design of an OO NOR gate, the required truth table, and the required Q-bar output and λ_0 operation.

very low loss cascade of OOL gates will be feasible. This section presents a generic or schematic way in which to implement OOL in the group-IV or III−V semiconductor integrated-photonic platforms. Details of the silicon-based group-IV method for PDs and disk EOM are given in the previous section. A primary motivation for developing the various gates is to have the ability to interconnect tens or hundreds or thousands of them seamlessly on one PIC chip in order to achieve a complex logic function and/or to improve the performance of an electronic digital computer using an integrated-photonics "section" within that computer.

According to the numerical results presented in the previous section, when designing the logic gates the following assumptions about the PDs and the EOM are made: (1) the disk is voltage-actuated and the wavelength shift of its resonance spectrum is quite linearly proportional to the applied voltage; (2) the logic level "1" of a digitally modulated optical input beam will produce PD photocurrent sufficient to give a photovoltage $V_{ph,1}$ across a load resistor that is connected directly across the two EOM terminals; (3) this $V_{ph,1}$ value will then cause a shift of the resonance spectrum that is 70% or more of the 3-dB resonance line width attained in the medium-Q or high-Q disk (see the previous section for detailed metrics); (4) the CW input beam to the OOL gate has optical power large enough at Q and Q-bar outputs to give modulated output bits whose optical power is 100% or more of the logic-1 input power.

Figure 7a shows the device for the first four gates. The PDs are reverse-biased PINs and the EOM is a reverse-biased PN depleter. In the second bus for the EOM, light couples in the reverse direction, but the 180-degree bend then sends light in the same output direction that the first bus does. A helpful property is that the logic pattern exiting the second bus Q-bar is the Q-logic inverse, the pattern complementary to the pattern exiting the first bus Q. The availability of complementary pulse trains helps to implement the first four gates.

Now let us look at the resonant optical transmission spectra of the Figure 7a gates, examining both Q and Q-bar. Because the two PD currents are added together in Figure 7a, we find from the possible, (0,0) and (0,1) and (1,0), (1,1) logic "combinations" that there will be generally three possible voltages driving the EOM: 0 V, $V_{ph,1}$, and $V_{ph,2}$, where $V_{ph,2}$ represents the photovoltage value inducing a resonance shift of about 2 times the disk line width. Therefore, those voltages will produce the three spectra illustrated in Figure 6c,d for the Q and Q-bar possibilities with the dip (peak) occurring at the wavelength of λ_0, or λ_1 or λ_2. Knowing these possibilities in Figure 6c,d, we can then look at the truth table of the desired gate and make a decision about the best wavelength of operation among our three choices. In other words, our choices are Q or Q-bar and λ_0 or λ_2. Proceeding in that manner, we obtain the four gates illustrated in Figure 7b−e. The XOR and XNOR logic outputs can be achieved by the same circuit by reading the Q-bar and Q outputs at λ_1, respectively (see Figure 8a,b). Of course, better ER occurs if a larger shifting rule is used, at the expenses of required electrical power. Finally, the simple logic OOL NOT gate with one

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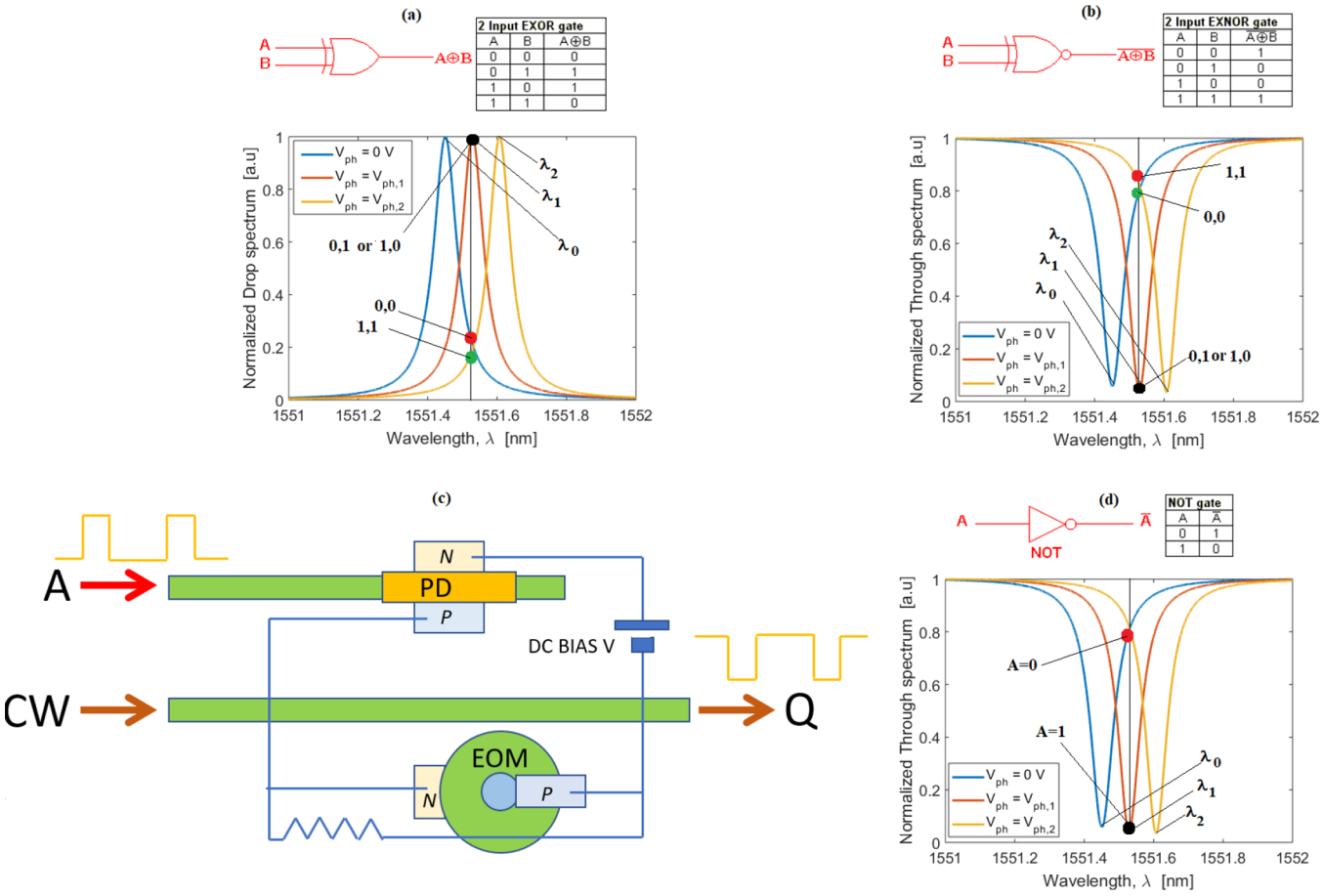

Figure 8. (a) Design of an OO XOR gate, the required truth table and the required Q-bar output and λ_1 operation; (b) Design of an OO XNOR gate, the required truth table, and the required Q output and λ_1 operation; (c) Schematic top view of proposed optical-to-electrical and electrical-to-optical NOT logic gate in a strip-waveguided photonic-integrated circuit; (d) Design of an OO NOT gate, the required truth table, and the required Q output and λ_1 choice.

optical input and one optical output can be seen in Figure 8c. Here there are two possible resonance spectra, one at 0 V and the other at $V_{ph,1}$, on the EOM. This leads to the performance shown in Figure 8d. Finally, the logic gate behavior requires that the optical signal power and the temperature are exactly fixed. Among these parameters, we think that the critical shortcoming is represented by the temperature change ΔT. For that reason, it is opportune to consider the OEO performance in the context of a silicon PIC, including the driver circuitry. As outlined in ref 6, the baseline temperature variations within a microprocessor are typically within ±5 °C. Over this range, the temperature-induced resonance shift could be estimated as 0.06 nm/°C.[6] In this context, the electro-optic tuning achieved by varying the bias voltage from the reverse-biased to the forward-biased regimes of operation could be large enough to compensate for thermal shifts in the range under investigation. For example, our investigations indicate that the resonance shift induced by a heating of about ΔT = +5 °C could be compensated by means of a forward-bias voltage of about 0.8 V (smaller values are obtained by increasing the doping levels). Thus, the proposed OEO devices require the inclusion of additional biasing circuitry that corrects for thermal effects.

DUAL-FUNCTION GATES

If we decide to use outputs Q and Q-bar simultaneously, then we discover double-purpose gates in Figure 7b–e and Figures 8a,b. One device offers two functions at the same time—specifically, AND and NAND from one device at the λ_2 wavelength, OR and NOR from one device at the λ_0 wavelength, and XOR and XNOR from one device at the λ_1 wavelength. In other words, OR is really OR/NOR, AND is AND/NAND and XOR is XOR/NOR. The idea here is to reduce the number of gates required to realize a specific complicated logic function by using Q/Q-bar gates. We have found reduction examples for AND/NAND.

Starting from logic input variables A,B,C,D, etc., Boolean theory says that any logic function, a particular and complicated logic output function of the various input variables, can always be obtained with a particular group of identical NAND that are joined together following a specific interconnection diagram, thereby forming an on-chip logic network or PIC. The same any-function result holds for identical NOR gates.

The ability to do "any" with "one type" of gate is favorable for OOL because it means that one wavelength of operation can be used for the entire system chip, whether it is NAND-based or NOR-based. In other words, both the A,B,C,D. . . light sources and the CW sources are at the same wavelength, λ_2 or λ_0, respectively.

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ONE WAVELENGTH FOR MIXED ARRAY

Unlike the one-type gate scenario just described, let us consider a network of different gate types. If we combine anywhere from two to six different types, then in order to construct a complicated logic-output function of several input variables, a problem arises with the wavelength of operation of the various gate-EOMs at their zero-volts-applied condition. This wavelength is different for the different types of gates (Figure 7b−e and Figure 8a,b). However, there is no problem for the various identical gate PDs because their broad-spectrum response gives equal photocurrents at λ_0, λ_1, and λ_2.

The solution to this EOM problem is to "tailor" the individual EOMs to a common purpose, which means that we adjust every EOM resonance wavelength at V = 0 to be aligned with the wavelength chosen for the entire chip. For example, if we choose λ_1 as the system wavelength for A,B,C,D and the CWs, and if we define $\delta\lambda$ as the wavelength separation between λ_0 and λ_1, and between λ_1 and λ_2, then, at V = 0, the resonance for AND EOMs is manufactured at $\lambda_1-\delta\lambda$, while the manufacturing gives the resonance at $\lambda_1+\delta\lambda$ for OR EOMs. The XNOR EOM is automatically at λ_1. Resonance tailoring could be done by disk radius control or by mechanical "trimming" of a cladding on the disk.

NUMERICAL SIMULATION METHOD

Our procedure is based on a multiphysics approach in which the FEM electromagnetic module that is used to evaluate the electric field distributions inside the SOI and PD waveguides, optical end-fire coupling, and photogeneration rate, works together with the FEM semiconductor module in order to simulate the PD behavior under the illumination condition. In this context, the carrier distribution as a function of voltage, simulated by FEM semiconductor module, was converted into an index distribution using the plasma dispersion (electro-refraction) equations.[36] The index distribution was fed into the FEM Electromagnetic module to determine the complex propagation constant as a function of voltage. The complex propagation constant was then inputted to the disk equation in order to theoretically predict the spectral response as a function of voltage. Let us now look at the doping profile, as induced by the ion implantation. In this context, several calculations were made to estimate the required dosages and implant energies for disk doping. In particular, the projected ranges, R_n and R_p, the straggles ΔR_n and ΔR_p and the implantation energy have been determined in order to obtain the desired doping profile. Range and straggle values are both functions of implantation energy and are found from experimental data for common acceptor and donor atoms implanted into silicon.[37] The results of this investigation indicate that boron can be implanted into the silicon at an approximated dose of 1.35×10^{13} cm^{-2} and energy of 60 keV. Similarly, phosphorus can be then implanted at an approximated dose of 7.2×10^{12} cm^{-2} and energy of 45 keV to create a p−n junction vertically centered in the disk. This induces the target doping level at the junction of around 4×10^{17} cm^{-3}. Moreover, the FEM semiconductor module has been used to estimate the modulator capacitance, including the full doping profile, the n+ and p+ regions and the depletion effect under reverse bias.

CONCLUSIONS

For operation at 1550 nm, an O-E-O device has been proposed for foundry implementation in the Group IV SOI/GeSn technological platform. For two optical inputs (one modulated, one CW), the cointegration of PD and EOM with suitable electrical bias-and-interconnect circuit, and load resistor, offers the possibility of realizing a photoreceiver without any electrical amplifier, an optical-amplifier-free optical repeater with gain, an optical wavelength converter (up or down), and a novel linear-optics realization of optical−optical logic gates such as AND, OR, NAND, NOR, XOR, and XNOR. This OOL is actually a higher-order version of the "3-terminal" OEO device because OOL gates have two optical logic signal inputs and two complementary logic outputs. Performing complicated logic functions appears feasible using interconnected gate arrays.

We identified the GeSn lateral PIN homojunction photoconductive PD as the high-performance PD that is compatible, electrically and optically, with the resonant Si vertical-PN-junction carrier-depletion EOM. We have derived here ion-implantation procedures that are optimum for realizing this EOM. Detailed simulations presented in this paper show that the information bandwidth for the photonic functions listed above is limited by the EOM capacitance (5 to 6 fF) appearing in the modulator-circuit RC time. An optical input power around 0.5 mW is needed to drive the OEO device, and a DC bias around 3 V is required for logic applications. The modulator extinction is 12 to 16 dB, with switching energy in the 5.8 to 9.6 fJ/bit range. A five-optical-beam OEOEEO device has been proposed for implementation in a semiconductor PIC as AND, OR, NAND, NOR, XOR, and XNOR optical−optical logic gates having two logic inputs and two complementary logic outputs. Because of the two simultaneous OE conversions of inputs at PDs and because of the immediate EO conversion of combined logic in an EOM powered by CW, the gated optical output can restore completely the logic-power levels of the optical inputs. For AND and OR, NAND and NOR gates, and XOR and XNOR, additive PD currents are used. An all-optical NOT gate is also proposed to achieve logic inversion via an OEO device. The factory-compatible PIC devices use strip waveguides, embedded PIN diodes and PN-depletion microdisk resonant EOMs side-coupled to strips. Rather than the traditional NLO approach, this is a linear-optics technique. Operating at one V = 0 wavelength, logic circuits composed of numerous different (or identical) interconnected gates appear feasible.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript. R.A.S. conceived the idea; F.D.L. developed the model and performed the simulations; and R.A.S., Z.Y., V.M.N.P., and R.T.C. supervised the work and gave critical reading and adjustments to the paper.

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Notes

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REFERENCES

(1) Nozaki, K.; Matsuo, S.; Fujii, T.; Takeda, K.; Shinya, A.; Kuramochi, E.; Notomi, M. Femtofarad optoelectronic integration demonstrating energy-saving signal conversion and nonlinear functions. *Nat. Photonics* **2019**, *13*, 454−459.

(2) Soref, R. Group IV photonics: Enabling 2 μm communications. *Nat. Photonics* **2015**, *9* (6), 358.

(3) Ying, Z.; Feng, C.; Zhao, Z.; Soref, R.; Pan, D.; Chen, R. T. Integrated multi-operand electro-optic logic gates for optical computing. *Appl. Phys. Lett.* **2019**, *115*, 171104.

(4) Li, Z.; Li, G. Ultrahigh-speed reconfigurable logic gates based on four-wave mixing in a semiconductor optical amplifier. *IEEE Photonics Technol. Lett.* **2006**, *18*, 1341−1343.

(5) Khorasaninejad, M.; Saini, S. S. All-optical logic gates using nonlinear effects in silicon-on-insulator waveguides. *Appl. Opt.* **2009**, *48*, F31−F36.

(6) Timurdogan, E.; Sorace-Agaskar, C. M.; Sun, J.; Hosseini, E. S.; Biberman, A.; Watts, M. R. An ultralow power athermal silicon modulator. *Nat. Commun.* **2014**, *5*, 4008.

(7) Gostimirovic, D.; Ye, W. N. Ultracompact CMOS-compatible optical logic using carrier depletion in microdisk resonators. *Sci. Rep.* **2017**, *7*, 12603.

(8) Chang, C.; Chang, T.-W.; Li, H.; Cheng, H. H.; Soref, R.; Sun, G.; Hendrickson, J. R. Room-temperature 2-Rm GeSn P-I-N homojunction light-emitting diode for in-plane coupling to group IV waveguides. *Appl. Phys. Lett.* **2017**, *111*, 141105.

(9) Soref, R.; De Leonardis, F.; Passaro, V. M. N. Simulations of nanoscale room temperature waveguide-coupled single-photon avalanche detectors for silicon photonic sensing and quantum applications. *ACS Appl. Nano Mater.* **2019**, *2*, 7503−7512.

(10) Cook, C. S.; Zollner, S.; Bauer, M. R.; Aella, P.; Kouvetakis, J.; Menendez, J. Optical constants and interband transitions of$Ge_{1-x}Sn_x$ alloys (x< 0.2) grown on Si by UHV-CVD. *Thin Solid Films* **2004**, *455*, 217−221.

(11) Kim, Y.; Fujikata, J.; Takahashi, S.; Takenaka, M.; Takagi, S. First demonstration of SiGe-based carrierinjection Mach-Zehnder modulator with enhanced plasma dispersion effect. *Opt. Express* **2016**, *24* (3), 1979−1985.

(12) Tran, H.; Du, W.; Ghetmiri, S. A.; Mosleh, A.; Sun, G.; Soref, R. A.; Margetis, J.; Tolle, J.; Li, B.; Naseem, H. A.; Yu, S. Q. Systematic study of $Ge_{1-x}Sn_x$ absorption coefficient and refractive index for the device applications of Si-based optoelectronics. *J. Appl. Phys.* **2016**, *119*, 103106.

(13) *COMSOL Multiphysics*, single license; COMSOL Inc.: Stockholm, Sweden, 2005.

(14) Gehl, M.; Long, C.; Trotter, D.; Starbuck, A.; Pomerene, A.; Wright, J. B.; Melgaard, S.; Siirola, J.; Lentine, A. L.; Derose, C. Operation of high-speed silicon photonic micro-disk modulators at cryogenic temperatures. *Optica.* **2017**, *4* (3), 374−382.

(15) Hosseini, E. S.; Yegnanarayanan, S.; Atabaki, A. H.; Soltani, M.; Adibi, A. Systematic design and fabrication of high-Q single-mode pulley-coupled planar silicon nitride microdisk resonators at visible wavelengths. *Opt. Express* **2010**, *18*, 2127−2136.

(16) Gardes, F. Y.; Brimont, A.; Sanchis, P.; Rasigade, G.; Marris-Morini, D.; O'Faolain, L.; Dong, F.; Fedeli, J. M.; Dumon, P.; Vivien, L.; Krauss, T. F.; Reed, G. T.; Martì, J. High-speed modulation of a compact silicon ring resonator based on a reverse-biased pn diode. *Opt. Express* **2009**, *17* (24), 21986−21991.

(17) Dong, P.; Liao, S.; Feng, D.; Liang, H.; Zheng, D.; Shafiiha, R.; Kung, C.-C.; Qian, W.; Li, G.; Zheng, X.; Krishnamoorthy, A. V.; Asghari, M. Low V_{pp}, ultralow-energy, compact, high-speed silicon electro-optic modulator. *Opt. Express* **2009**, *17* (25), 22484−22490.

(18) Arlotti, C.; Almuneau, G.; Gauthier-Lafaye, O.; Calvez, S. Coupled mode analysis of micro-disk resonators with an asymmetric-index-profile coupling region. *Proc. SPIE* **2017**, *10090*, 100901D.

(19) Zhang, L.; Ji, R.; Jia, L.; Yang, L.; Zhou, P.; Tian, Y.; Chen, P.; Lu, Y.; Jiang, Z.; Liu, Y.; Fang, Q.; Yu, M. Demonstration of directed XOR/XNOR logic gates using two cascaded microring resonators. *Opt. Lett.* **2010**, *35* (10), 1620−1622.

(20) Hardy, J.; Shamir, J. Optics inspired logic architecture James. *Opt. Express* **2007**, *15* (1), 150−165.

(21) Miller, D. A. B.; Chemla, D. S.; Damen, T. C.; Gossard, A. C.; Wiegmann, W.; Wood, T. H.; Burrus, C. A. Novel hybrid optically bistable switch: The quantum well selfelectrooptic effect device. *Appl. Phys. Lett.* **1984**, *45* (1), 13−15.

(22) Ying, Z.; Zhao, Z.; Feng, C.; Mital, R.; Dhar, S.; Pan, D. Z.; Soref, R.; Chen, R. T. Electronic-photonic arithmetic logic unit for high-speed computing. *Opt. Express* **2018**, *26*, 28002.

(23) Ying, Z.; Feng, C.; Zhao, Z.; Soref, R. A.; Pan, D. Z.; Chen, R. T. Integrated multi-operand electro-optic logic gates for optical computing. *Appl. Phys. Lett.* **2019**, *115*, 171104.

(24) Ying, Z.; Zhao, Z.; Feng, C.; Mital, R.; Dhar, S.; Pan, D. Z.; Soref, R.; Chen, R. T. Automated logic synthesis for electro-optic logic-based integrated optical computing. *Opt. Express* **2018**, *26* (21), 28002−28012.

(25) Zhao, Z.; Gu, J.; Ying, Z.; Feng, C.; Chen, R. T.; Pan, D. Z. Design Technology for Scalable and Robust Photonic Integrated Circuits. *2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4−7, 2019; IEEE, 2019; pp 1−7.

(26) Alkabani, Y.; Miscuglio, M.; Sorger, V. J.; El-Ghazawi, T. OEO-CAM A Hybrid Opto-Electronic Content Addressable Memory. *IEEE Photonics J.* **2020**, 1.

(27) Shor, P. W. Algorithms for quantum computation: discrete logarithms and factoring. *Proceedings 35th Annual Symposium on Foundations of Computer Science. IEEE Comp. Soc. Press* **1994**, 124−134.

(28) Xu, Q.; Soref, R. Reconfigurable optical directed-logic circuits using microresonator-based optical switches. *Opt. Express* **2011**, *19* (6), 5244−5259.

(29) Tian, Y.; Zhang, L.; Xu, Q.; Yang, L. XOR/XNOR directed logic circuit based on coupled-resonator-induced transparency. *Laser Photonics Rev.* **2013**, *7* (1), 109−113.

(30) Zhang, L.; Ding, J.; Tian, Y.; Ji, R.; Yang, L.; Chen, H.; Zhou, P.; Lu, Y.; Zhu, W.; Min, R. Electro-optic directed logic circuit based on microring resonators for XOR/XNOR operations. *Opt. Express* **2012**, *20* (11), 11605−11614.

(31) Qiu, C.; Ye, X.; Soref, R.; Yang, L.; Xu, Q. Demonstration of reconfigurable electro-optical logic with silicon photonic integrated circuits. *Opt. Lett.* **2012**, *37* (19), 3942−3944.

(32) Ying, Z.; Wang, Z.; Zhao, Z.; Dhar, S.; Pan, D. Z.; Soref, R.; Chen, R. T. Silicon microdisk-based full adders for optical computing. *Opt. Lett.* **2018**, *43* (5), 983−986.

(33) Ying, Z.; Dhar, S.; Zhao, Z.; Feng, C.; Mital, R.; Chung, C.-J.; Pan, D. Z.; Soref, R. A.; Chen, R. T. Electro-optic ripple-carry adder in

integrated silicon photonics for optical computing. *IEEE J. Sel. Top. Quantum Electron.* **2018**, *24* (6), 1−10.
(34) Ying, Z.; Zhao, Z.; Feng, C.; Mital, R.; Dhar, S.; Pan, D. Z.; Soref, R. A.; Chen, R. T. Automated logic synthesis for electro-optic logic-based integrated optical computing,. *Opt. Express* **2018**, *26*, 28002−28012.
(35) Li, F.; Vo, T. D.; Husko, C.; Pelusi, M.; Xu, D.-X.; Densmore, A.; Ma, R.; Janz, S.; Eggleton, B. J.; Moss, D. J. All-optical XOR logic gate for 40Gb/s DPSK signals via FWM in a silicon nanowire. *Opt. Express* **2011**, *19* (21), 20364−20371.
(36) Soref, R.; Bennett, B. Electrooptical effects in silicon. *IEEE J. Quantum Electron.* **1987**, *23*, 123−129.
(37) Sze, S. M.; Ng, K. K. *Physics of Semiconductor Devices*, 3rd ed.; John Wiley & Sons, 2006.

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