

Silicon photonic subspace neural chip for hardware-efficient deep learning

Chenghao Feng^{1,2,6}, Jiaqi Gu^{2,6}, Hanqing Zhu², Zhoufeng Ying^{1,3}, Zheng Zhao^{1,4}, David Z. Pan^{2,*}, Ray T. Chen^{2,5,*}

¹Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758, USA.

²Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas 78705, USA.

³Alpine Optoelectronics, CA, USA.

⁴Synopsys Inc., CA, USA.

⁵Omega Optics, Inc., 8500 Shoal Creek Blvd., Bldg. 4, Suite 200, Austin, TX 78757, USA.

⁶These authors contributed equally.

*Corresponding authors: chenrt@austin.utexas.edu, dpan@ece.utexas.edu

As deep learning has shown revolutionary performance in many artificial intelligence applications, its escalating computation demand requires hardware accelerators for massive parallelism and improved throughput. The optical neural network (ONN) is a promising candidate for next-generation neurocomputing due to its high parallelism, low latency, and low energy consumption. Here, we devise a hardware-efficient photonic subspace neural network (PSNN) architecture, which targets lower optical component usage, area cost, and energy consumption than previous ONN architectures with comparable task performance. Additionally, a hardware-aware training framework is provided to minimize the required device programming precision, lessen the chip area, and boost the noise robustness. We experimentally demonstrate our PSNN on a butterfly-style programmable silicon photonic integrated circuit and show its utility in practical image recognition tasks.

Deep neural networks (DNNs) have demonstrated superior performance in various intelligence tasks, such as image recognition, decision making, and language translation¹⁻⁴. Hardware accelerators capable of performing high-speed, energy-efficient, and parallel multiply-accumulate (MAC) operations are in high demand with the rapidly-escalating DNN model size and data volume. However, electronic digital hardware accelerators, including but not limited to graphical processing units (GPUs), field-programmable gate arrays (FPGAs)⁵, and other digital application-specific integrated circuits (ASICs)⁶⁻⁸, are inevitably limited by millisecond-level latency, high energy consumption, excessive heat, and high interconnect cost^{9,10}. In contrast, analog neuromorphic computing represents a paradigm shift in efficient DNN acceleration, significantly increasing parallelism and energy efficiency¹¹⁻¹³.

The optical neural network (ONN) is a promising analog artificial intelligence (AI) accelerator that features low latency, wide bandwidth, and high parallelism of light^{14–19}. Earlier work has presented a range of high-performance integrated photonic neural networks that implement multi-layer perceptrons (MLPs)^{14,20,21} or convolutional neural networks (CNNs)^{22,23}. The fundamental matrix-vector multiplication (MVM) unit is realized using Mach-Zehnder interferometer (MZI) arrays or microring-resonator (MRR) arrays. By tuning the phase shifters in MZIs or the transmission of MRRs, these photonic systems are designed to implement universal linear operations or general matrix multiplication (GEMM) with a relatively high requirement in device control precision. Recent studies show that the construction of DNNs can move beyond conventional GEMM with restricted matrix parameter space, e.g., low-rank NNS^{24–26}, structured NNS^{27–29}, which shows not only considerable hardware efficiency improvement but also comparable representability to classical GEMM-based NNS. We refer to such NN architectures as subspace neural networks. The success of such a design concept can be reproduced in ONNs by trading the universality of weight representation for higher hardware efficiency. Several structured ONNs have been proposed to reduce the number of optical components, e.g., the fast-Fourier-transform-based (FFT-based) ONN^{29–31}. In this work, we further explore this “subspace” NN design concept in the optical domain and experimentally demonstrate a novel photonic subspace neural network (PSNN) with superior hardware efficiency and compactness.

Additionally, noise-tolerant ONN training currently still lacks an efficient, scalable, and physically-evaluated solution. As is the case with other analog computing platforms, ONNs will inevitably encounter performance degradation or even malfunction due to non-ideal factors, e.g., process variations^{32,33}, limited control precision^{21,34}, and dynamic noises³⁵. Recently, on-chip training has become an appealing trend towards noise-resilient ONNs. Numerous on-chip training algorithms have been proposed to directly optimize optical devices with in-situ noise handling^{36–41}. However, prior ONN on-chip training protocols suffer from algorithmic inefficiency and require costly hardware overhead, e.g., phase detection³⁶, high-resolution optical component control³⁷, or per-device field monitoring^{36,41}. Therefore, applying them to practical ONN training is still technically challenging.

In this work, we propose a PSNN for next-generation hardware-efficient deep learning. Our proposed PSNN partitions each layer’s weight matrix into smaller $k \times k$ ($k=4,8$) submatrices with restricted parameter space. Our architecture can achieve photonic neural computing with $7\times$ fewer trainable optical components compared to MZI-based ONN architectures designed for general MVMs⁴², resulting in a $2.1\times$ smaller footprint and $5.5\times$ lower

latency. The number of trainable optical components can be further reduced by $\sim 70\%$ using structured circuit pruning⁴³ with negligible ($<0.2\%$) task performance loss. Moreover, an efficient and scalable hardware-aware training framework is experimentally deployed to enable ONN training with high noise robustness and low control precision requirement. Our PSNN is then experimentally demonstrated on a butterfly-style photonic integrated circuit (BPPIC) and evaluated on the MNIST hand-written digits classification task⁴⁴ with a measured accuracy of 94.16%. Our performance analysis reveals that our PSNN can achieve a computational density of 1689 tera (10E+12) operations per second/mm² (TOPS/mm²) and energy efficiency of >10 TOPS/W using compact optical devices, e.g., microdisk-based active devices⁴⁵. Our proposed photonic subspace neural network architecture and hardware-aware training framework provide a synergistic solution that unleashes the power of optics from a novel co-design perspective and pushes the limits of next-generation efficient AI.

Results

Photonic subspace neural network

The proposed PSNN and its training framework are depicted in Fig. 1. The mathematical representation of one layer in a typical DNN with n inputs and m outputs is shown in Fig. 1(b), along with its hardware implementation shown in Fig. 1(c). Here we partition the $m \times n$ weight matrix \mathbf{W} into $m^* \times n^*$ submatrices $\{\mathbf{W}_{i,j} \in \mathbb{C}^{k \times k}\}_{i \in [n^*], j \in [m^*]}$. The input vector \mathbf{x}_{in} is encoded as the amplitude of the optical signals and will also be partitioned into n^* segments $\mathbf{x}_{in} = (\mathbf{x}_{in}^1, \mathbf{x}_{in}^2, \dots, \mathbf{x}_{in}^{n^*})$. Thus, the MVM operation can be expressed using the block matrix multiplication formula as follows,

$$\mathbf{x}'_{out} = \mathbf{W}\mathbf{x}_{in} = \begin{pmatrix} \sum_{j=1}^{n^*} \mathbf{W}_{1,j} \mathbf{x}_{in}^j \\ \sum_{j=1}^{n^*} \mathbf{W}_{2,j} \mathbf{x}_{in}^j \\ \vdots \\ \sum_{j=1}^{n^*} \mathbf{W}_{m^*,j} \mathbf{x}_{in}^j \end{pmatrix}. \quad \text{Eq. (1)}$$

Each submatrix $\mathbf{W}_{i,j}$ can be decomposed as $\mathbf{W}_{i,j} = \mathbf{B}\mathbf{\Sigma}_{i,j}\mathbf{P}$, where \mathbf{B} and \mathbf{P} are both $k \times k$ unitary matrices shown in Fig. 1(d), and $\mathbf{\Sigma}_{i,j}$ is a $k \times k$ diagonal matrix. As illustrated in Fig. 1(e), we use two programmable photonic integrated circuits (PICs), namely, a butterfly-style transform unit (\mathbf{B} unit) and a projection unit (\mathbf{P} unit), to implement the unitary matrices \mathbf{B} and \mathbf{P} using phase shifters, directional couplers, and waveguide crossings.

The diagonal matrix unit $\Sigma_{i,j}$ is composed of k amplitude modulators and k phase shifters for amplitude and phase tuning, respectively.

One critical property of PSNN is that the \mathbf{B} and \mathbf{P} units can flexibly support multiple unitary transforms. Once the desired states of \mathbf{B} and \mathbf{P} units are accomplished by tuning the phase shifters in them, they will not be modified throughout the training and mapping processes, leaving only the $\Sigma_{i,j}$ units trainable. As a result, the total number of trainable optical devices is $\frac{2mn}{k}$ in an n -input, m -output layer, considerably reducing the weight loading cost and reprogramming complexity. As depicted in Fig. 1(d), several commonly used structured neural networks can be realized by configuring the phase shifters in \mathbf{B} and \mathbf{P} units. For example, a block-circulant matrix can be realized (Fig. 1(d(1))) when the \mathbf{P} unit performs optical FFT while the \mathbf{B} unit performs optical inverse FFT (IFFT)²⁷. Furthermore, our \mathbf{B} and \mathbf{P} units can execute Hadamard transformation (HT), which can be used to achieve efficient DNN inference⁴⁶. (Detailed phase configurations can be found in supplementary Notes 1 and 2). Figure 1(d(2)) shows the matrix pattern when both \mathbf{P} and \mathbf{B} units implement HT. The superior versatility of PSNN also supports a wide range of unitary transforms for neural computing with other phase configurations, e.g., leave all phase shifters untuned, which will be demonstrated experimentally hereinafter.

Another essential property of our PSNN is that different $\Sigma_{i,j}$ units can share the \mathbf{B} and \mathbf{P} units, leading to significant chip area reduction. Since all $\mathbf{W}_{i,j}$ s are constructed by the same \mathbf{B}, \mathbf{P} transforms, \mathbf{B} and \mathbf{P} units can be reused in the optical domain. Here, we rewrite Eq. 1 with matrix multiplication's distributive and associative properties:

$$\mathbf{x}'_{out} = \mathbf{W}\mathbf{x}_{in} = \begin{pmatrix} \Sigma_{j=1}^{n^*} \mathbf{B}\Sigma_{1,j}\mathbf{P}\mathbf{x}_j \\ \Sigma_{j=1}^{n^*} \mathbf{B}\Sigma_{2,j}\mathbf{P}\mathbf{x}_j \\ \vdots \\ \Sigma_{j=1}^{n^*} \mathbf{B}\Sigma_{m^*,j}\mathbf{P}\mathbf{x}_j \end{pmatrix} = \begin{pmatrix} \mathbf{B}\Sigma_{j=1}^{n^*}\Sigma_{1,j}\mathbf{x}_j \\ \mathbf{B}\Sigma_{j=1}^{n^*}\Sigma_{2,j}\mathbf{x}_j \\ \vdots \\ \mathbf{B}\Sigma_{j=1}^{n^*}\Sigma_{m^*,j}\mathbf{x}_j \end{pmatrix}, \quad (\text{Eq. 2})$$

where $\mathbf{x}_j = \mathbf{P}\mathbf{x}_j$. By sharing the unitary matrix units, one can implement an MVM operation of size $m \times n$ with only m/k \mathbf{P} units and n/k \mathbf{B} units, dramatically reducing the footprint of the PSNN compared to previous FFT-based ONN architecture, which requires $\frac{mn}{k}$ \mathbf{P} and \mathbf{B} units³⁰. The mechanism of the optical architecture shown in Fig. 1(b) can then be stated as follows: First, the input optical signal \mathbf{x}_{in} is partitioned into n^* segments \mathbf{x}_j s and then propagate through the \mathbf{P} units to generate \mathbf{x}_j s, which will then be distributed via a fanout network to $m^* \times n^*$

diagonal matrix units $\Sigma_{i,j}$ s. After propagating through the $\Sigma_{i,j}$ units, the signals will be combined and fed into each B unit with a combiner network to obtain the MVM result. Finally, as with all typical NN architectures, a nonlinear activation unit (σ unit) is required to generate the output of the layer x_{out} , which has been realized by all-optical non-linear devices or optoelectronic circuits in previous work^{47,48}. We omit details on this.

Hardware-aware training framework

After manufacturing, fabrication variances in optical components and dynamic noises will introduce uncertainty into the ONN. What is more, the numerical resolution of implementable weight matrices is limited by the precision of electrical signals used to program the ONN. Consequently, the task performance will deteriorate. To remedy this noise robustness issue, we build a multi-stage hardware-aware training framework.

The general procedures of the training framework are shown as follows: First, the PSNN is calibrated on-chip to measure the performance of tunable components and prepare the state of the photonic chip to approach the desired transfer matrix. In reality, the actual transfer matrix of the photonic neural chip deviates from the designed one due to performance variations of the optical components, e.g., the unbalanced splitting ratio of directional couplers. Second, to model the non-ideal behavior and predict the response of the real optical neural chip, we develop an NN-based differentiable PIC estimator (DPE) using measurement data and AI algorithms. The third step involves determining the DNN parameters and mapping them to the electrical control signals using a hardware-aware training and parameter mapping process. The DPE is used to efficiently emulate the real chip response to facilitate training. Quantization-aware training with dynamic noise injection techniques is used to improve the noise tolerance with limited device control resolution. Thus, our PSNN can achieve the performance target despite control precision restrictions and other non-idealities. Compared with prior in-situ or on-chip training protocols based on derivative-free optimization algorithms^{14,38,49,50}, our AI-assisted ONN learning flow shows considerably higher scalability and effectiveness in robust optical neural chip training.

Experiment

In this work, we experimentally demonstrate the practicality of the PSNN on the silicon photonics platform using a butterfly-style programmable PIC (BPPIC) capable of implementing 4×4 $\mathbf{B}\Sigma\mathbf{P}$ blocks in our PSNN. The layout of the chip was drawn and verified using Synopsys OptoDesigner, while the chip was fabricated by the Advanced Micro Foundry (AMF). The basic optical components of the BPPIC, such as phase shifters, 50-50 directional couplers, crossings, are depicted in Fig. 2(b). The unitary matrix units \mathbf{B}/\mathbf{P} are marked in red/green in Fig. 2(d). The active phase shifters in these regions support enough flexibility to realize different unitary transforms, but note that they are not optimized as parameters during ONN training. The diagonal matrix unit (Σ unit) is built using an array of MZI attenuators for magnitude and phase control⁵¹.

The schematic of the testing setup is shown in Fig. 2(a). To eliminate the phase fluctuations of optical signals in off-chip fibers, which have been reported in other work⁵², CW light of different wavelengths is coupled in different input grating couplers separately. Besides, phase detection at the outputs can be avoided when light beams of different wavelengths are used as inputs⁵⁰ (More detailed explanations are provided in Supplementary Note 3). The input modulators and phase shifters of the BPPIC are programmed by a high-precision multi-channel digital-to-analog converter (DAC). Off-chip photodetector arrays will collect the output signals, which will subsequently be read using oscilloscopes or analog-to-digital converters (ADCs). A microcontroller is used to write electrical signals to the DAC and read the output signals in this work. The measurement data are processed by computers to train and implement the DNN model. It should be noted that current fabrication and packaging technologies enable the integration of electrical circuits, photodetectors, and the laser on a single chip⁵³ with potentially much higher compactness, shorter interconnect path, and higher efficiency. The experimental setup is described in detail in Methods.

Here we experimentally implement the multi-stage hardware-aware training flow on our BPPIC. In the calibration stage, the performance of modulators and phase shifters in the BPPIC are first calibrated individually, such that we can precisely control the state of active devices, especially the input modulators and the Σ matrix (The calibration results are detailed in Supplementary Note 4). The second stage is to learn desired device configurations via ONN training. We first program the BPPIC with representative input signals and phase shifter control voltages and collect the corresponding outputs. The above measured input-output pairs are used to train a differentiable circuit model for accurate and efficient non-ideality modeling. Then, we embed this model into our

ONN training procedure as an ultra-fast, accurate, and differentiable PIC simulator to effectively enable hardware-aware training. Quantization-aware training and dynamic noise injection techniques are used during training to adapt the ONN model to limited phase shifter control resolutions and boost the PIC robustness to dynamic system noises.

In this work, we construct a CNN with our BPPIC and benchmark its performance on a hand-written digits classification dataset MNIST⁴⁴. We use MVM operations to implement CNNs with a widely-applied tensor unrolling method (im2col)⁵⁴, as detailed in Supplementary Note 5. Figure 3(a) illustrates the network structure. Here, large-size tensor operations are partitioned into 4×4 blocks and mapped onto our BPPIC. The partial product accumulation and non-linear activation functions, e.g., ReLU, are simulated on computers. Figure 3(b) visualizes multiple output images after being convolved by learned kernels. The confusion matrix depicting the prediction results of hand-written digit recognition is also shown in Fig. 3(c). When the voltage control resolution is set to 3-bit (8 attenuation levels for each MZI attenuator in the Σ unit), the inference accuracy of the CNN reaches 94.16% in our experimental demonstration, slightly below the simulated value of 94.59%. More testing results are included in Supplementary Note 6, where we compare the accuracy of PSNN with different control voltage ranges and control resolutions. They will also be discussed in the following section.

Discussion

Footprint. Our PSNN outperforms SVD-based MZI ONN architectures¹⁴ in the number of trainable devices and the footprint. Rather than deploying area-costly MZI arrays, we use smaller optical components such as directional couplers, phase shifters, and crossings to construct the unitary matrix units \mathbf{B} and \mathbf{P} . The second reason that leads to our superior compactness is that many Σ units share the \mathbf{B} and \mathbf{P} units. As a result of massive hardware reuse, when the matrix size is 32×32 , our 8-point PSNN consumes $\sim 2.2 \times$ fewer phase shifters and $\sim 3.6 \times$ fewer directional couplers, leading to $\sim 2.1 \times$ area reduction compared to SVD-based MZI ONN architectures¹⁴ with the same matrix size and optical components. See the detailed evaluation of the chip area in Supplementary Note 7.

The chip area or hardware cost of PSNN can be further optimized with structured circuit pruning strategies. In an n -input, m -output layer, the $\frac{mn}{k^2}$ diagonal matrix units can be treated as $\frac{mn}{k^2}$ parameter groups. When all of the

transmission coefficients in one Σ unit are zeros, this unit or parameter group is unnecessary and can be omitted in PSNN designs. When training the DNN, penalty terms encouraging higher sparsity can be added to the training objective, allowing for the elimination of unneeded Σ units while minimizing task performance degradation. Our simulation results indicate that more than 70% of neural connections in our PSNN can be pruned with negligible (<0.2%) accuracy loss when implementing image recognition tasks such as MNIST⁴⁴ or FashionMNIST⁵⁵. (Results are provided in Supplementary Note 7). On these datasets, our pruned PSNN can save around 70% of trainable optical components, resulting in ~52% chip area reduction.

Computational speed and energy efficiency. Our PSNN utilizes light to implement MVM operations, which outperforms electronic counterparts in both speed and energy efficiency. Taking into account the delay contributed by high-speed modulators (10 ps)^{45,56}, photodetectors (10 ps)⁵⁷, ADCs (100 ps)⁵⁸, and the optical path (46.5 ps), the total delay required to implement a 32×32 MVM can reach ~166.5 ps, which corresponds to an operating frequency of around 6 GHz. Using the same component library⁵⁹, the propagation delay of the optical path in our PSNN is $5.5 \times$ less than that of an MZI-based ONN¹⁴. The computational speed of PSNN is now constrained by optical-to-electrical (OE) or electrical-to-optical (EO) conversion, but it can be increased further by using all-optical devices as non-linear activation functions⁴⁰ (See Supplementary Note 8).

The total power consumption of PSNN for MVM operations is comprised of the power to drive the laser/modulators/photodetectors, the power to set the weight matrix, and the power to drive the ADCs. Numerous energy-efficient active optical components have been developed in recent years. For instance, the silicon microdisk modulator achieves approximately 1 fJ per bit⁶⁰. Maintaining the weight matrix takes less than 2.5 mW per phase shifter in our AMF-manufactured neural chip, which can be decreased to zero by setting weights with phase change materials or nano-opto-electro-mechanical devices^{61,62}. Concerning the power consumption of ADCs, despite the availability of high-speed ADCs, the power consumption of ADCs is significantly higher than that of other components. For example, an 8-bit, 40 GSPS ADC consumes 200 mW per channel, while an 8-bit, 10 GSPS ADC consumes 39 mW per channel⁵⁸. Thus, the operating speed, the matrix size n , and the block size k determine the energy efficiency of PSNN, which is about 9.6 TOPS/W for a 32×32 8-point PSNN operating at 6.0 GHz. The detailed performance analysis is given in supplementary materials Note 9 and 10.

In addition, the number of trainable devices in our k -point PSNN is only $\mathcal{O}\left(\frac{mn}{k}\right)$, which saves energy for storing and reconfiguring weights. In comparison to ONN architectures designed for general MVM, where the number

of programmable devices is around $\mathcal{O}(mn)^{20}$ or $\mathcal{O}(\max(m^2, n^2))^{14}$, the memory cost of storing and accessing the weight matrix and the energy required to reconfigure corresponding active devices are also reduced by k times. This feature of PSNN will bring considerable energy efficiency improvement when weights need to be reconfigured frequently in large-scale DNNs, where weight loading takes nontrivial hardware cost even with weight-stationary dataflow⁶³.

Resolution analysis. Our PSNN is capable of achieving a high accuracy under low-bit control of optical components. Prior ONN architectures designed for general MVMs require high-precision control of optical devices for parameter mapping to maintain accuracy¹⁴. Otherwise, we may encounter severe task performance degradation because of large mapping errors⁶⁴, which will quickly accumulate as the size of weight matrices or the number of layers increases. Given that the control precision of some energy-efficient photonic tensor cores is only 4 or 5 bits²¹, it is necessary to reduce the resolution requirement of ONN architectures and enhance the tolerance of quantization errors. In this study, quantization-aware training is applied to our PSNN to adopt the limited voltage control precision and mitigate the accuracy loss. In experiments, we have shown that $\sim 95\%$ accuracy can be achieved for digit recognition when the precision of the DACs for controlling the phase shifters is around 3-bit (See Supplementary Note 6). What is more, low-resolution device control can also lessen the energy cost for weight storage, access, and reconfiguration⁶⁵.

Robustness. The robustness of our PSNN is guaranteed by our hardware-aware training framework. Our AI-assisted DPE provides accurate variation modelling of static noises, e.g., process variations, device calibration errors, thermal crosstalk, and non-ideal extinction ratio of modulators. Besides, our noise-injection training algorithm further considers the impacts of dynamic noises, e.g., thermal noises from the laser source and photodetection noises. The robustness of our architecture is evaluated by varying the signal-to-noise-ratio (SNR) of the inputs and the phase drifts of phase shifters in MZI attenuators, and our analysis results are shown in Fig. 3(d). Thanks to our noise injection techniques, our PSNN maintains greater than 90% average inference accuracy even when the standard deviation of input noise and phase drifts reach 0.1 and 0.2, respectively.

Additionally, the robustness of our PSNN can be enhanced with more reliable optical components and more reliable control circuits⁶⁶. For bandwidth-driven and robustness-driven PSNN design, one can directly select

broadband MZI with low temperature sensitivity as a robust variable optical attenuator (VOA). Less robust but more compact or energy-efficient components can also be employed, e.g., ultra-compact MRR modulators with on-chip feedback controls and PCM-based modulators with advanced high-endurance materials.

Scaling and outlook. The performance metrics of the PSNN can be further improved in several directions. First, our PSNN is compatible with the majority of the device-level enhancement techniques. For example, by using smaller directional couplers⁶⁷, crossings⁶⁸, and VOAs⁶⁹, the chip area of the PSNN can be optimized, resulting in a competitive computing density of 1689 TOPS/mm² and energy efficiency of >10 TOPS/W (See Supplementary Note 11). Second, massive multiplexing techniques can substantially boost the throughput of our architecture. Because all of the optical components in our architecture can be broadband devices, wavelength-division multiplexing (WDM) techniques can be applied to our architecture: If k -wavelength input signals propagate through the chip simultaneously to implement the MVM in parallel, the throughput and the computing density can then be improved by $(k-1)$ times over a single-wavelength PSNN. Furthermore, more circuit structures and optical components can be investigated to construct our PSNN. Notably, the BPPIC is not the only option to implement $\mathbf{B}\mathbf{\Sigma}\mathbf{P}$. For example, recent work demonstrates that multiport n -to- n directional couplers or multimode interference (MMI) couplers can be utilized to build unitary matrices⁷⁰ and they can also be used to build the \mathbf{B} and \mathbf{P} unit to reduce the chip area. Finally, faster or more energy-efficient EO/OE conversion techniques are demanded to improve the computational speed and energy efficiency for data movement between electrons and photons, which currently restricts the performance of optical computing platforms.

Conclusion

We present a hardware-efficient photonic subspace neural network (PSNN) architecture with experimental demonstrations on a silicon photonic programmable butterfly-style photonic integrated circuit (BPPIC). By exploring optical neurocomputing beyond conventional GEMMs with restricted weight representability, our PSNN consumes up to $7\times$ fewer trainable optical components than prior MZI-based ONN architectures designed for GEMMs. This advantage can be further increased to $\sim 23\times$ using structured circuit pruning strategies with negligible accuracy loss. Our proposed hardware-aware training framework efficiently models the behavior of the PSNN to help reduce control precision requirement, enhance noise robustness, and fully exploit the expressivity in the subspace. The performance of PSNN can be further improved with smaller optical components as well as faster and more efficient EO/OE conversion techniques. Our PSNN pushes the limits of scalability and the

robustness of ONNs and creates a new design paradigm for next-generation high-performance AI accelerators with improved hardware efficiency.

Methods

Chip implementation and testing. The photonic chip layout of BPPIC was developed and verified in Synopsys Optodesigner. The chip was fabricated by Advanced Micro Foundry (AMF). 40 DC pads are designed for tuning the phase shifters and the modulators on the neural chip, which are wire-bonded to a printed circuit board (PCB). Here we configure the phase shifters on the BPPIC using a 40-channel 14-bit DAC (AD5370), which is controlled by a microcontroller (Raspberry Pi 4). The phase shift is programmed by solving for $\Delta\phi = \gamma V^2$, where γ is the tuning factor of the phase shifter and is calibrated before the on-chip training. Similarly, the transmission of the MZI modulators are altered by solving $T(V) = \cos\left(\frac{\phi(V)}{2}\right) e^{-j\left(\frac{\phi(V)}{2} + \frac{\pi}{2}\right)}$, where $\phi(V) = \gamma_1 V_1^2 - \gamma_2 V_2^2 + \phi_b$ denotes the phase difference between the two modulation arms, γ_1 and γ_2 are the tuning factors of the two modulation arms, while V_1 and V_2 are the operating voltages. ϕ_b denotes the phase difference when no voltages are applied on the modulation arms. Both the magnitude and phase of the diagonal matrix unit can be programmed with V_1 and V_2 .

A 10-channel standard single-mode fiber array (SMF28) was employed to couple light into and out of the BPPIC through grating couplers. The fiber array was attached to the optical neural chip to avoid intensity fluctuations of the input light beams. In the testing, the transmission spectrum of the PSNN is measured with broadband amplified spontaneous emission (ASE) lasers from Thorlabs and optical spectrum analyzers (OSA) from AssetRelay. The measurement results show that the coupling efficiency of our chip is approximately 10 dB at 1550 nm. A tunable laser from ID Photonics was used for generating continuous wave (CW) light. The output optical signals were coupled out and converted to electrical signals using four InGaAs switchable gain amplified detectors (Thorlabs PDA10CS2). The voltage signals will be read by two oscilloscopes (Digilent analog discovery 2), which are controlled by the microcontroller (Raspberry Pi 4). With the application programming interface (API), one can access the DAC and obtain the results from the oscilloscope in one program.

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Author contributions. C. F., J. G. designed the floorplan and drew the layout. C. F. built the experimental setup and performed the measurements. J. G. developed codes for training the optical neural chip. H. Z., Z. Y., and Z. Z. assisted in verifying the architecture and designing the chip. C. F. and J. G. conceived the architecture and wrote the manuscript with contributions from R.T. C., D.Z. P. R.T. C. and D.Z. P. led the project.

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Data availability. The data that support the findings of this study are available from the corresponding author upon reasonable request.

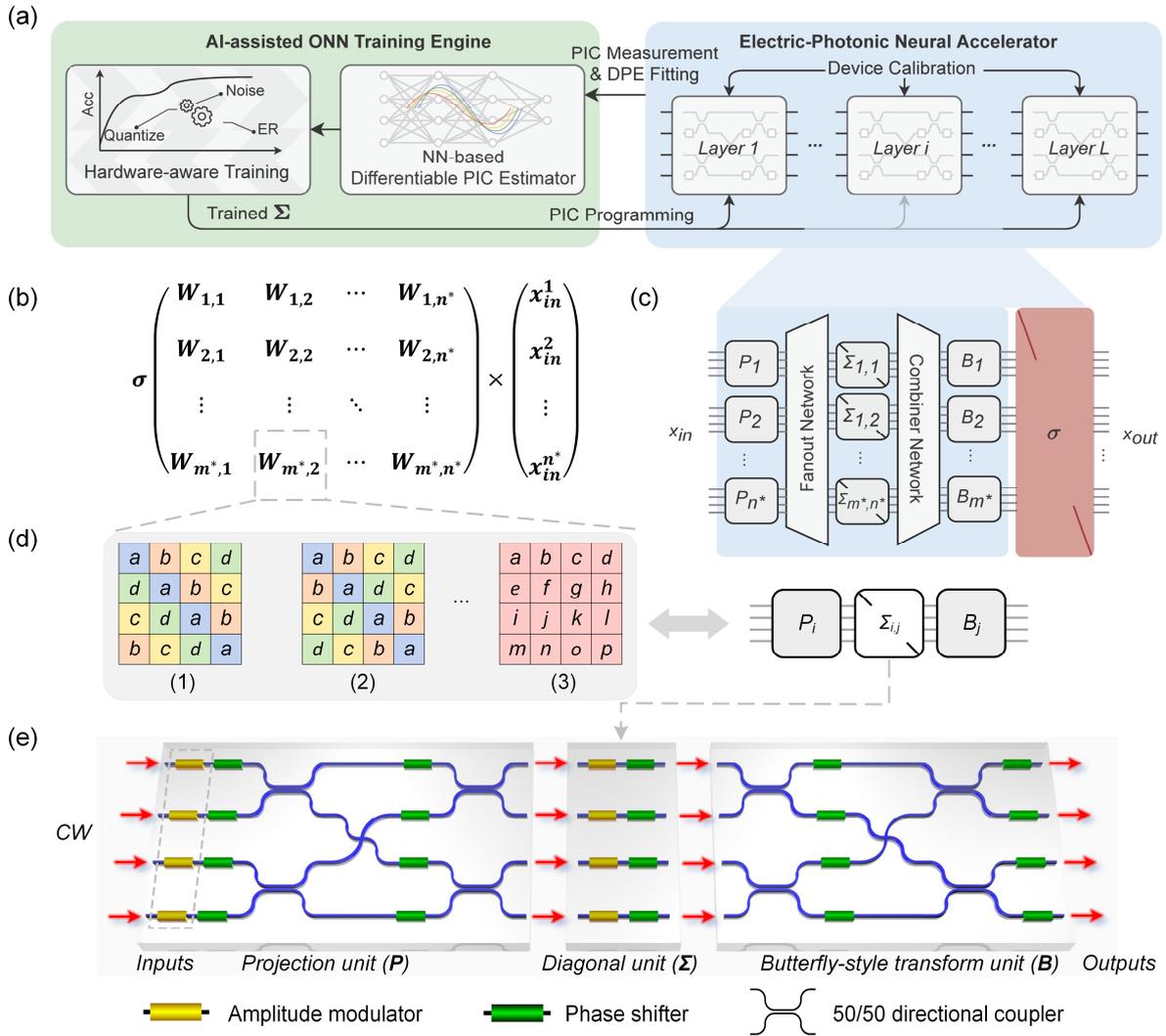


Fig. 1 General architecture of the photonic subspace neural network (PSNN). The hardware-aware training framework is shown in (a). The mathematical representation of one layer in our PSNN is shown in (b), where an $m \times n$ matrix is partitioned to $\frac{mn}{k^2}$ blocks. The hardware representation of one layer is shown in (c), which consists of $n^* = \frac{n}{k}$ projection units (**P** units), $m^* = \frac{m}{k}$ butterfly-style transform units (**B** units), $m^* \times n^*$ diagonal matrix units (Σ units). The fanout network and the combiner network are used to distribute and combine the optical signals to different optical paths. By setting phase shifters in **B** units and **P** units, several popular structured ONNs based on (1) Fast Fourier transform and inverse Fast Fourier transform, (2) Hadamard transform, or (3) other implementable transforms are shown in (d). (e) Schematic of 4×4 **B**, **P**, and Σ units, respectively, which are the building blocks of a 4-point PSNN. To train the PSNN, we first perform an on-chip device calibration on our PSNN. The measurement data are learned and modeled in our hardware-aware training flow. Besides, other factors such as the precision of controlling signals, limited extinction ratio (ER) of input modulators, and other noises are also considered in our training engine to improve the accuracy and robustness of our PSNN.

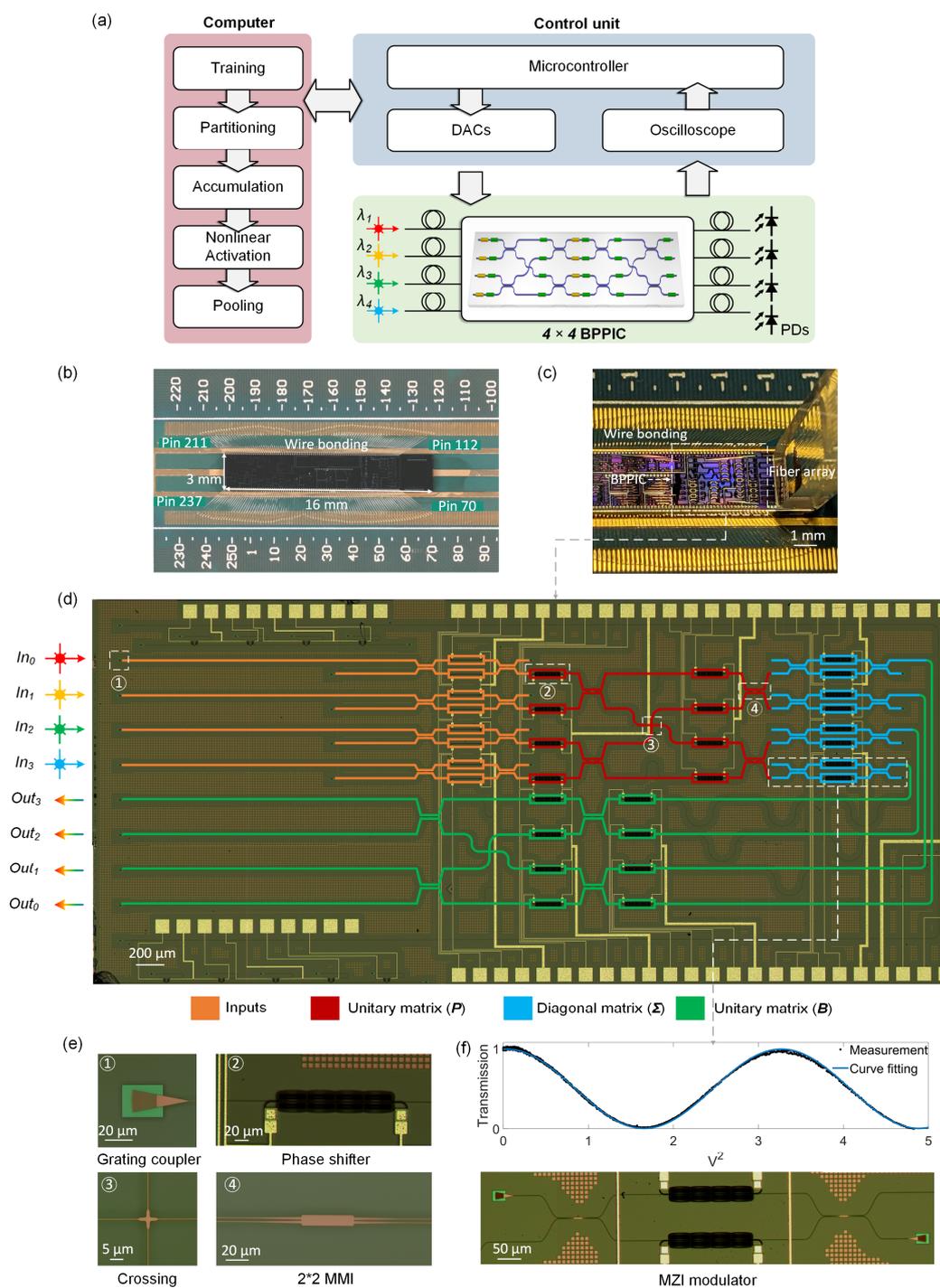


Fig. 2 Experimental demonstrations of PSNN. (a) Schematic of our PSNN experiment setup. The entire MVM is first partitioned into multiple 4×4 blocks, and each block is implemented optically on a butterfly-style PIC (BPPIC). (b) shows the wire-bonded photonic chip and its starting/ending electrical pin numbers, while (c) is the photography of the chip testing setup. The micrograph of the BPPIC is shown in (d). The input optical beams with different wavelengths are shown in different colors. The necessary optical components are highlighted in (e). (f) shows the schematic and the normalized transmission curve of an MZI attenuator in the diagonal matrix unit (Σ unit). Only the attenuators in Σ are programmed in training. The parameters and the input signals are programmed by a multi-channel digital-to-analog converter (DAC), while the output signals are read by the oscilloscope. Both the oscilloscope and the DAC are controlled by a microcontroller. The MVM results are provided to the computer for data processing in order to train and deploy the DNN.

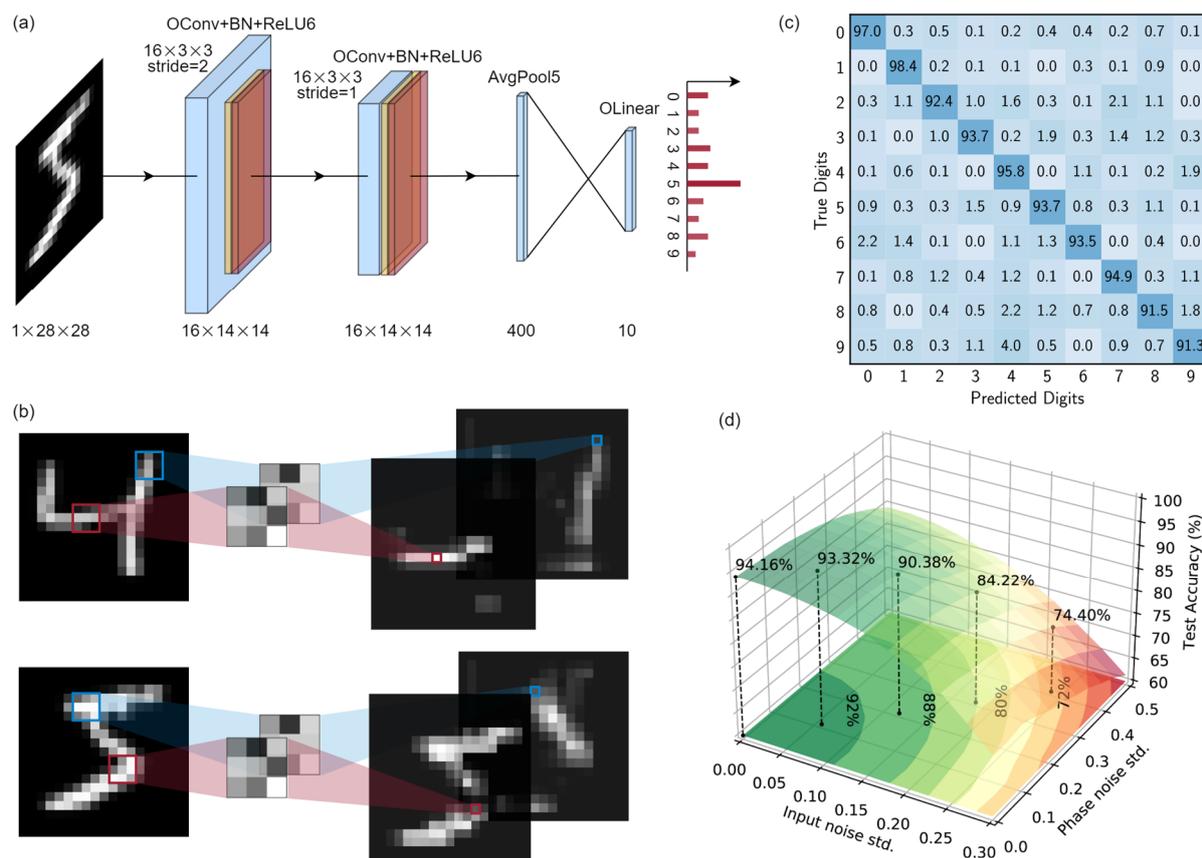


Fig. 3 Digit recognition with our PSNN. (a) Structure of the CNN, the convolution is realized by PSNN with im2col approach. The first convolutional layer has one input channel and 16 output channels with a stride of 2. The subsequent convolutional layer has 16 input/output channels with a stride of 1, and the size of the convolutional kernel is 3×3 . After adaptive average pooling, we have $5 \times 5 \times 16 = 400$ hidden features, followed by a linear classifier with 10 outputs. (b) Experimental results of convolving two input images with convolution kernels of size 3×3 in our PSNN. (c) The confusion matrix of the trained PSNN on MNIST, showing a measured accuracy of 94.16%. (d) Robustness analysis of the PSNN. Dynamic noises are injected into the inputs and phase shifters in PSNN, and the variations of accuracy are shown accordingly.