High-throughput optoelectronic interconnect for holographic memory devices

Bipin Bihari*[a], Jinghuai Fa[a], Xuegong Deng[a], Brian M. Davies[b], Suning Tang[b] and Ray T. Chen[a]

[a]Microelectronics Research Center, University of Texas at Austin, Austin, TX 78758

[b]Radiant Research, Inc., 3006 Longhorn Blvd., Suite 105, Austin, TX 78758

ABSTRACT

Novel optical memory systems (such as holographic memory system) offer ultra large storage capacity and with fast access time. The current commercial system can produce in access of 300 Mb/s aggregate data rate and near future system will yield aggregate data rates on the order of 1-10 Gb/s. However, full exploitation of this feature is possible only if memory to processor interface is fast enough to handle such a data rate. In this presentation, a unique optoelectronic interconnect architecture based on WDM and WDDM are described.

Keywords: Optoelectronics, WDM, WDDM, Guided-wave, Optical Storage

1. INTRODUCTION

Optical storage systems and memories are emerging rapidly as a solution to address the next generation requirement of high data-density and of fast access time. In particular, three-dimensional memories such as two-photon and holographic storage systems have the potential to provide high throughput rate, high storage capacity and high parallelism[1-6]. These specific attributes of optical storage systems are particularly important for applications involving image processing because of their potential to provide parallel processing over hundreds of images, thereby keeping up with the flow of images coming in from various sensing nodes at an ultra-high speed. In the past few years, we have witnessed considerable effort to implement optical-data storage technologies and to create a commercially successful data storage product based on these technologies[7,8]. Recent developments in constituent component technologies such as liquid-crystal displays (LCD) and solid-state detector arrays suitable for holographic storage data input and output devices make the effort more realistic. The most attractive feature, the fast access of the entire stored data in the optical memory device, results from the intrinsic page-oriented parallel access. This feature along with the ability to store multiple holograms in a small volume of storage medium, offers the potential of very high throughput rates. If the full response of the holographic volume is utilized, a very high data density on the order of 10^{11} bit/cm^3 or greater is feasible. However, full exploitation of developments in new three-dimensional memory systems will require handling of the aggregate data rates on the order of 1-10 Gb/s or more at a distance above 10 cm. One of the issues in this scenario is the appropriate interconnection between memory device and processing unit. Conventional electronic transmission lines fail to provide require bandwidth for handling such high data rates. Furthermore, technologies for constructing low-power, lightweight, efficient, and low-cost devices and components with significantly improved performance are required. Electrical interconnect systems fail to meet these requirements due to their basic limitations, which make the employment of optical components a necessity. Optical components inherently offer advantages of high-speed data carrying capacity and ultra-high data density. However, high cost, complex processing, and coupling and integration bottlenecks are the prime hurdles to be removed before optical technology can be fully utilized to its maximum potential.

We are developing an optoelectronic interconnect based on WD(D)M technology (wavelength division (de)multiplexing) which can provide high speed and bi-directional transport of signals between the optical memory devices and processor boards. This interconnect will utilize polymer-based guided-wave devices in conjunction with multimode optical fiber/ fiber arrays and wavelength division (de)multiplexers (WD(D)M).

In this innovative research effort, we intends to solve all the above mentioned problems by combining advantages of WDM, polymer-based photonic devices, and state-of-the-art micro-fabrication techniques to make waveguide optical components and tapered channel waveguides to provide cost-effective, reliable, and low-loss propagation of optical signals and efficient input and output coupling among the arrays of optoelectronic devices and optical-fiber arrays. The schematic view of the optoelectronic system connecting processors and memories is shown in Fig. 1. The parallel data obtained from the memory device can be converted into the optical signal by an array of multi-wavelength lasers. A waveguide grating or mirror coupler will be used to couple this light signal into an array of channel waveguides converging into a single output and

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therefore fulfill the wavelength division multiplexing. The channel waveguides can be mode-matched with both single-mode and multimode optical fibers to transmit the optical signal to the processor (receiver) end. At the receiver end, a wavelength division demultiplexer (WDDM) can be incorporated to demultiplex the optical signal. The demultiplexed optical signals can be converted into electrical signals with a photodiode array. The implementation of this optoelectronic interconnect system will reduce the latency of data transfer between memory and processors. This scheme also requires only one fiber for parallel data transmission, and thereby reduces the complex optical alignment. The optical transmission channel can be either an optical fiber or a thin-film waveguide depending on the interconnection distance.

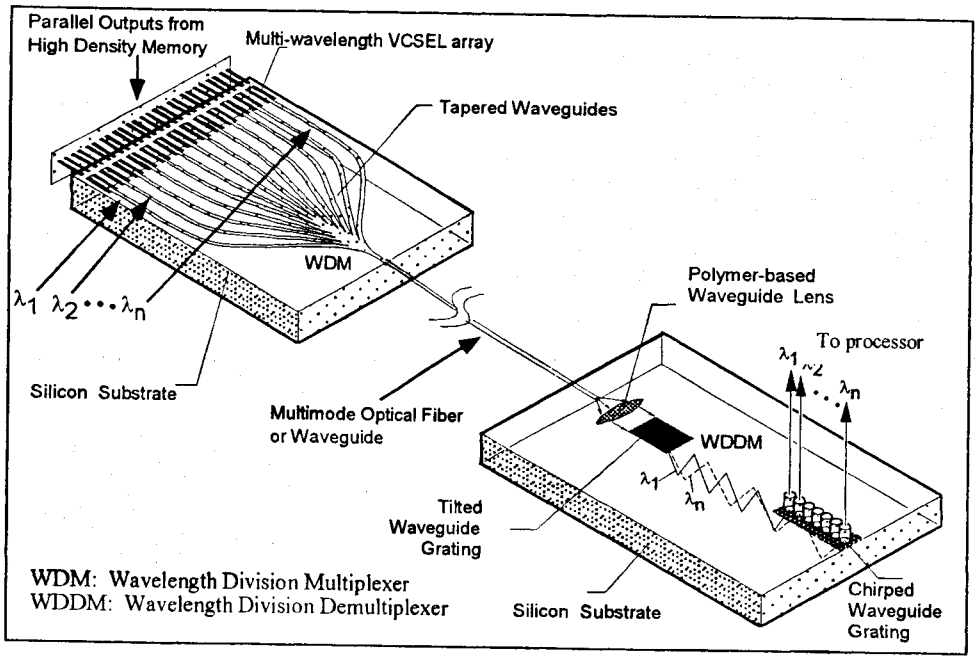


Fig. 1 Schematic of the proposed interconnect system.

To date no finalized-standard exists for optical interconnects to fulfill the high-speed interconnection requirements at the data-com level. Optoelectronic interface standards being developed for American National Standards for Information Technology such as HIPPI-6400-OPT have promise as a viable solution to the bottleneck arising from the large aggregate data rate to be handled. The HIPPI-6400-OPT specifications can serve as the guidelines for any device in this scenario.

Several key technologies including low-loss optical fiber arrays, VCSEL arrays, and photodiode arrays are required for the realization of optoelectronic interconnection for high-speed data transport. The impediments, which need to be removed before these novel technologies are made available to the industry, include efficient optical coupling from one device to another to obtain reasonably low-power performance at reasonable costs and a standard protocol to interface the memory devices to the processor network or user. In the optical specifications for the latest version of HIPPI-6400-OPT interface standards, the coupling losses at the optical interfaces are still an open question under investigation and revision[9]. This bottleneck is mainly a consequence of the mode mismatch when two devices having different shape and sizes of the output and input ports are coupled together. This makes it necessary to find an intermediate coupling device, which can eliminate the mode mismatch problem. The polymeric waveguides and waveguide-couplers certainly can bridge this missing link. A properly designed tapered waveguide in conjunction with an efficient waveguide grating/mirror coupler can provide an adiabatic transition of optical signal from one device to another having different mode sizes without excessive insertion losses, which will make low-power operation feasible.

2. HOLOGRAPHIC OPTICAL DATA STORAGE SYSTEMS

The end devices to be considered here include a holographic memory that can produce several Gbits/sec aggregate data rates on the one side and the processing devices on the other. In a holographic memory system, the information is recorded in a photo-refractive medium in the form of a spatial interference pattern. Two coherent laser beams, one carrying the spatial information called "object beam" and the other "reference beam" propagating in a particular direction are mixed together to generate the hologram. Illuminating the recorded hologram with the reference beam will yield or reconstruct the object beam

and vice versa. As the holographic material becomes thicker, the reconstruction becomes very sensitive to the particular angle of incidence of the reference beam, which allows multiple objects to be recorded in the same volume and accessed independently by using an appropriate set of associated reference beams. Such holograms can be recorded sequentially, each object beam illuminating the holographic material simultaneously with its unique reference beam. Several thousand holograms can be multiplexed and stored in 3.0 cm^3 of $Fe:LiNbO_3$ crystal. To read the stored holographic information, the object beam is turned off, allowing only the reference beam to focus on the photo-refractive medium. The reference beam's location is determined by the particular pages to be read. The beam illuminates the interference grating stored at this location, resulting in the reconstruction of the original data pattern. An imager that converts the pattern signal back to electronic data in a holographic memory system reads the pattern. The first commercial holographic memory system developed by Holoplex (HM-100) stores up to 1000 images, each consisting of 640 x 480 pixels with an access time of about one second. Recent demonstrations have shown that more than 10,000 holograms can be multiplexed in a common volume. Each page potentially can hold 1 Mbit of information, and the parallel retrieval of single page in a time interval of 100 μs is possible (the detector array response time). A system with above specifications will yield a data transfer rate of 10 Gb/s[10]. Next generation holographic memories will require aggregate data transfer rates well above 10 Gb/s to fully exploit its potential where large volume and fast access of information are needed. However, the conventional electronic transmission lines or interconnects can not keep up with this kind of aggregate data rates even beyond a few cm of the line length. There is no interconnection system available in the industry at present that can handle such a data rate. The bit parallel optical interconnects as described here can circumvent these problems.

2.1 Parallel Output from Reading Device (CCD Array)

There are a number of imager options which can be used in the optical memory devices. These options differ in the method of photon sensing and the method of transferring charge from the pixel to the external interface. The most favored imager option at present is a CCD (charge-coupled device). The CCDs are essentially rows of analog pixel cells interconnected with analog shift registers. Multi-phase (2,3, or 4-phase) clocks are used to bias the silicon substrate, pushing charge along the register. Other imager options are the RAI (Random Access Imager) and CID (Charge Injection Devices). A detailed description of the mechanism involved in these devices is irrelevant here. However, it is important

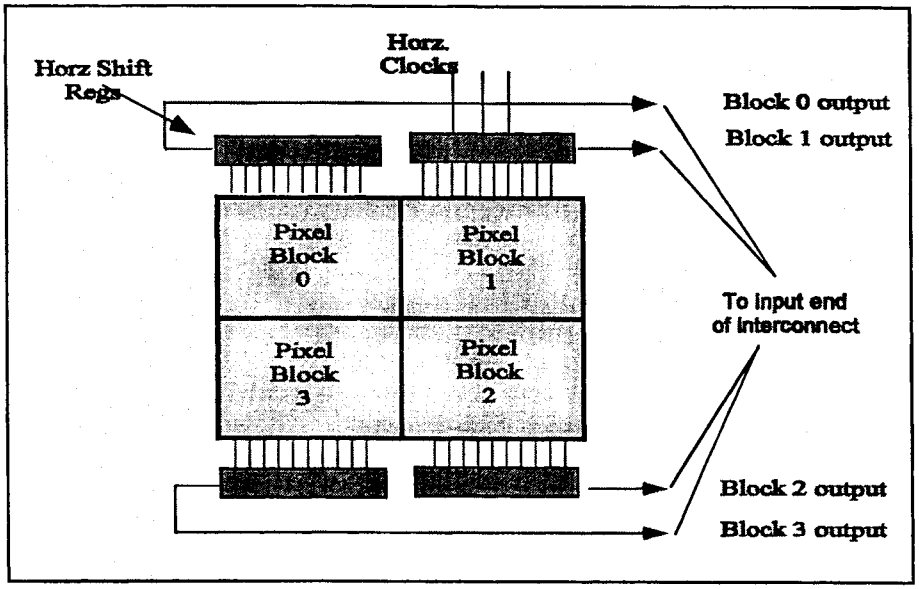


Fig. 2. Multi-tap output from memory device to external interface.

to note that in all of these devices the data rate may be limited by the ability of the device to shift data through CMOS analog shift registers. Current CMOS design rules indicate that analog shift speed of several tens of MHz is possible. The digital shift speed can be in excess of 60-80 MHz. However, the common solution to pixel shift-speed limitations is to use multiple output lines. This can be facilitated by segmenting the two-dimensional pixel array into blocks with an analog shift register for each block (Fig. 2), and read out these blocks of the CCD array in parallel with multiple-output channels. Each block in this configuration is read in a serial manner. Due to space considerations and convenience of the CCD design, shift registers in this configuration typically flow data outwards from the center of the CCD. The system impact of this is that pixel data

must be flipped around in memory and/ or merged with other quadrants to reconstruct the original data pattern. In return, aggregate pixel speeds far in excess of those supported in CMOS silicon can be achieved.

3. THE TARGETED SYSTEM ARCHITECTURE

High quality computer image/video systems are comprised of three core parts: the volume storage system to store the information, a high speed transmission system to retrieve and transmit the image/video from memory, and the computer system to process and playback the information. The storage part of the system may consist of one or several high-density optical memories. Holographic memory systems provide a possibility of huge volume of data storage in conjunction with fast retrieval of the stored data. In order to exploit its full potential, high-speed transmission between server and consumer is required.

The information consumer at the computer end focuses on two kinds of usage. One is the store-process system type, where, received information can be stored in main memory first, and then is processed by a CPU. The main memory electronic storage-speed, to keep up with optical transmission speed at the receiver, still needs a breakthrough in technology, unless we directly connect the CPU with optical memory. However, direct CPU and optical memory connection suffers the efficiency problem since instruction set deals with data set in a short burst style (i.e. it will not be the same as large volume image retrieve where read operation overrules the write, and information flow is in the steady style). Another information consumer type at the computer end is the real-time image/video architecture, where the incoming information is not necessarily stored in the main memory. Instead, the information is sent directly to display equipment in real time. Volume storage and high-speed transmission may play a more important role in this architecture. The two architectures connecting the holographic memory and a server node are shown schematically in Fig. 3.

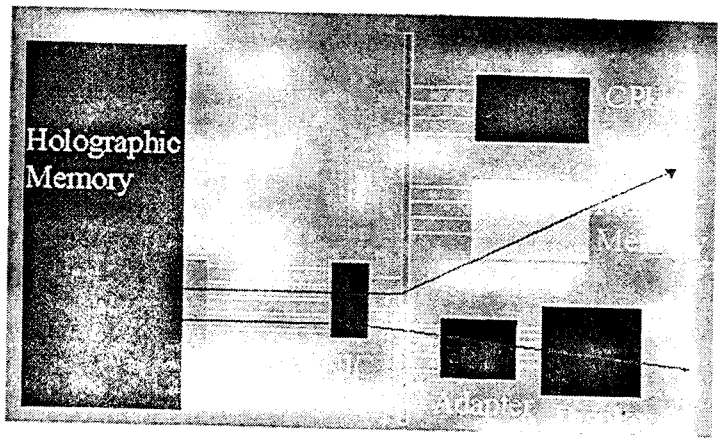


Fig. 3. General architecture of interconnection between holographic memory and processor

Bit-parallel transmission can be realized using the WDM technology. It is a point to point interconnection contrasting with BUS structure. Several server nodes can be interconnected through a switching device. The optical fibers can support the transmission speed of thousands of GHz. High-speed digital circuit or flip-flop element can be used to overcome the electrical bottleneck on the server side for RAM access or on the holographic memory side for CCD access.

On the server side, CPU, main memory, and display equipment are attached to the system bus, and the network interface card (NIC) interfaces received bit-parallel transmission signals with a system bus. Before a CPU can process data from optical memory, the data should be placed in the main memory (RAM). Otherwise, the data from holographic memory can be consumed directly by the display equipment. Both server side and optical memory side need high speed buffers to temporally hold part of the high speed information flow. The static RAM (SRAM) and the dynamic RAM (DRAM) are the two techniques used as buffer memory. SRAM technology uses flip-flop logic such as TTL, ECL, BiCMOS, SOI, Gallium Arsenide, etc., and can provide higher speed. On the other hand, DRAM uses electronic charge principles and can provide higher density but slower speed. SRAM in PC reaches up to the speed of 500 MHz, and in high end supercomputers it reaches up to 1-2 GHz. Thus, for 8 bit-parallel channels, memory throughput will be limited to 8 - 16 GHz with current technologies. For digital circuits, a 40 Gbit/s flip-flop IC has emerged through InP HEMT processing, but is not mature[11]. Only small size logic devices and buffers are achievable.

Here, we consider only a simple interconnection between holographic or high-throughput optical memory and one computer node. No switching for the networking is considered for simplicity, and in order to reduce inner delay within computer node, we omit the peripheral bus and adopt a single optical bus architecture. The following building blocks are necessary in order to realize a technically feasible and commercially viable interfacing of high throughput and fast access holographic or other emerging parallel optical memories, using polymer-based waveguide devices and WDM/WDDM technologies.

1. **WDM waveguide module.**
2. **WDDM module.**
3. **Transmission medium (optical fibers/channel waveguides)**
4. **Electrical to optical signal conversion (transmitter)**
5. **Optical to electrical conversion (receiver)**
6. **Hardware/software protocol and device drivers**

In the following we will discuss the development of optical hardware components and delineate some of the basics of software implementation issues.

4. WDM WAVEGUIDE AND OPTICAL COUPLING COMPONENTS

The WDM waveguide structure shown in Fig. 1 will perform the WDM (wavelength division multiplexing) function in the proposed interconnection system. On the input side of the waveguide structure, the optical signal from the WDM laser source (e.g. multi-wavelength VCSELs) will be coupled into different channels of waveguide converging into a single output port. The output end will be interfaced with the transmission line, which could be an optical fiber or waveguide depending on the interconnection hierarchy. For an acceptable integration of the guided-wave optics and existing electronic devices, waveguides must be Si-CMOS process compatible. Other important considerations include low-propagation loss, minimum insertion loss, easy manufacturing process and low cost. We have developed novel polymeric channel waveguides in conjunction with waveguide input and output couplers, which can address the above issues. Our approach will utilizes low-loss polyimides for optical channel waveguides, which are Si-CMOS process compatible, and all associated components including waveguides, waveguide-grating couplers, and waveguide splitters can be easily integrated and planarized if required.

The fabrication of polyimide-based 2-dimensionally-tapered waveguide structures as shown in Fig. 1, acting as a many to one WDM device (many-to-one coupler) is a trivial exercise of photolithography process. However, the vertical tapering in the waveguide can not be obtained using photolithography techniques. We have developed a compression molding technique that can be employed to construct the 3-dimensionally tapered waveguides of desired shapes and sizes. This technique is highly cost effective, when large number of devices are required.

Efficient input and output coupling is an important factor to be addressed for reasonable performance from the optoelectronic interconnects. We have polymer-based tilted waveguide gratings and 45^{o} total internal reflection based waveguide-mirror as potential approaches. While both the approaches can be used to couple the optical signal surface-normally into and out of a channel waveguide, planarization could be a challenging factor for a mirror based approach. In the interconnect scenario where no further layers are to be fabricated over the optical layer, the 45^{o} waveguide mirror has obvious advantage of high coupling efficiency and ease of fabrication considering the fact that in this particular scenario planarization may not be a strict requirement. On the other hand, the grating coupler will be a choice for intermediate layer optical interconnects as reasonable degree of efficiencies could be achieved along with the advantage of ease of planarization. Fig. 4 shows a photograph of tilted-profile rectangular grating as an input-grating coupler on glass

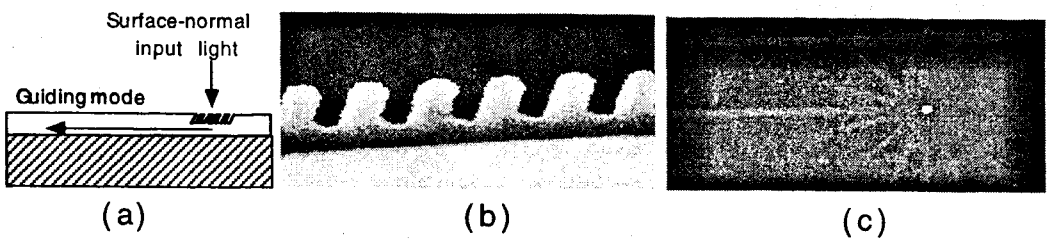


Fig. 4. (a) The schematic of a surface-normal input coupling using tilted grating. (b) SEM micrograph of polyimide grating with tilt angle of ~32°. (c) The photograph of coupling a surface-normal input laser into the polyimide waveguide.

substrate. A theoretical exercise indicates that an efficiency as high as 70% is achievable by using high index polyimides and fine tuning the grating parameters such as grating period, depth, and tilt angles. The waveguide mirror-coupler is the 45^0 slanted end surface of the polyimide waveguide. The optical signals can be coupled in or out from the polyimide waveguides through the couplers surface-normally due to total internal reflection. One of the advantages of a mirror based coupler is its insensitivity to wavelength variations and therefore it can work for a wide range of wavelengths. Fig. 5 is a CCD camera picture of a waveguide mirror coupler showing the input coupling function. The mirror structure is fabricated using photolithography and RIE etching technique.

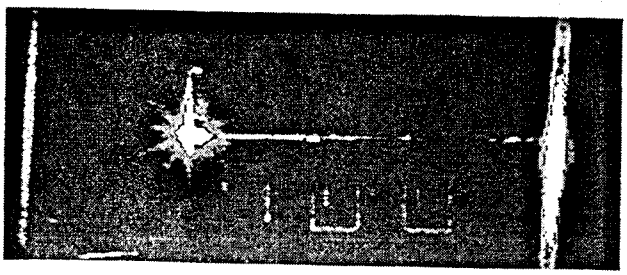


Fig. 5. A planar polyimide waveguide with waveguide mirror

4.1 Tapered waveguide as mode matching device:

The coupling loss at the optical interfaces is one of the major problem in optoelectronic interconnects. This bottleneck is mainly a consequence of different shape and size of constituent components required to realize such an interconnect system. Output and input ports of individual components are optimized in general for their own performance and result in a mode mismatch when two different devices are coupled. This makes it necessary to find an intermediate coupling device, which can eliminate the mode mismatch problem. Our approach to use a tapered waveguide structure is a step forward in this direction. The Fig. 6. a side view revealing the basic structure of a 3D-tapered polymer-based coupling device that can be employed, for example, to improve the optical coupling between a single-mode waveguide and a multi-mode waveguide[12].

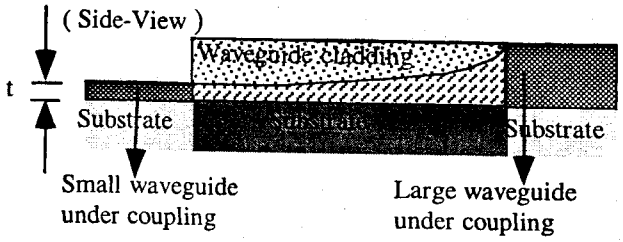


Fig. 6. Schematic of the tapered waveguide that can be used to improve the optical coupling efficiency between a small waveguide device and a large waveguide device.

5. WDDM FOR RECEIVING PARALLEL DATA

Wavelength division demultiplexing (WDDM) devices are key elements for enhancing the transmission bandwidth of the optical interconnect scenario presented here. During the past 20 years, various types of WDMs and WDDMs have been proposed and demonstrated, but many of these have just a few channels, are extremely expensive, or are designed for multiple independent channels in long-distance communications networks, where time skew between signals is unimportant[13,14]. For applications where data must be transmitted in a bit-parallel fashion and it is critical to maintain the synchronization between signals sent over separate parallel channels, since the parallel pulses represent bits in an n-bit byte, where n is the number of wavelength channels. This would require keeping the length of the fibers equalized, which is difficult in practice. A possible work-around to this time-skew problem is to send the signals along the same fiber, but on different wavelengths. By travelling over the same fiber, the delay in arrival of the pulses at the other end of the fiber can be compensated because the signal dispersion (as a function of wavelength) is a known quantity which depends on the fiber type and its length. Small variations in length and connectorization quality do not affect the relative signal delay. However, the WDDM must be chosen carefully. Those types of WDDM which are constructed of fiber Bragg gratings are not adequate for this purpose because, in practice, the lengths of the fibers used (and hence the delays of each wavelength signal) vary from device to device, and each device would have to be individually calibrated and compensated by a custom-built delay line array.

Our solution to this problem of uncontrollable skew among parallel channels in some types of WDDM is to use spatially multiplexed phase gratings recorded in polymer-based waveguide holograms. The relative delays (time skew) introduced here are well-characterized, repeatable, and can be compensated easily. Unlike electrical interconnects, WDM-based optical interconnect systems do not have an industrial standard to set the operation protocol governing the wavelength separation, except for the 1550 nm band used for very-long distance telecommunications, which has been standardized by the ITU. WDM wavelengths have not yet been standardized for the shorter-wavelength bands around 750-850 nm, for which multimode fiber is used for shorter distance links such as campus networks, Gigabit Ethernet, etc. Multiple fiber ribbon arrays and bundles will use multimode fiber, and hence we concentrate on this type of fiber for our initial WDDM design.

5.1 Four-Channel WDDM prototype

The schematic of the designed 4-channel WDDM using volume holographic grating and substrate guided-wave is shown in Fig. 7. The device was laid out on an optical table as shown in the Fig. 8 and optical signals was sent through the device

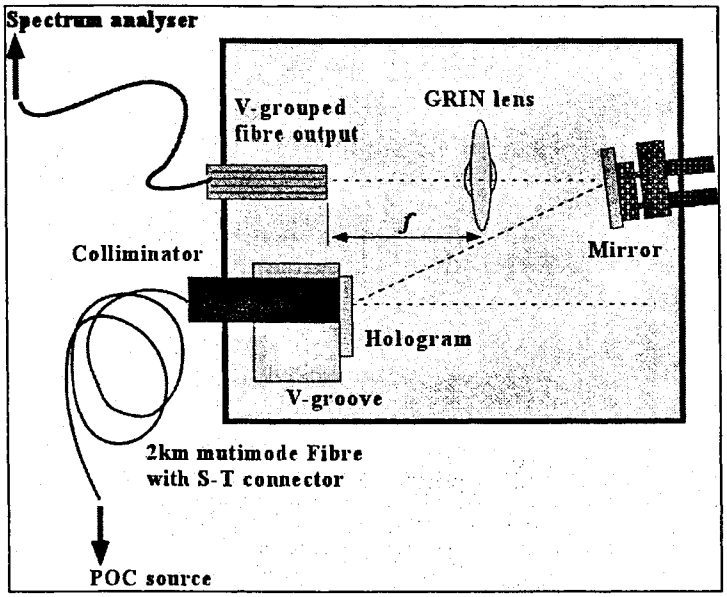


Fig.7. A 4-channel WDDM using volume holographic grating and substrate guided-wave.

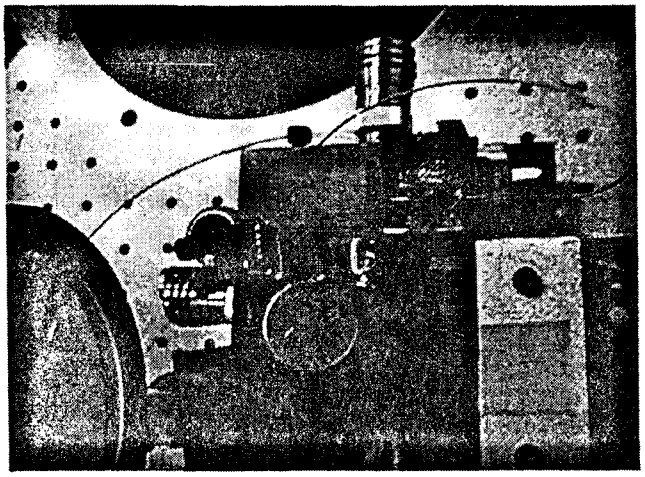


Fig. 8. Picture of the 4-channel WDDM device laid out on an optical table-top.

and into an Optical Spectrum Analyzer in order to characterize the alignment procedure. Optical signals were measured using an Optical Spectrum Analyzer, model AQ-6312B, from Ando. The input is taken from a multimedia transmitter, operating on 4 wavelengths, measured as 750, 780, 810, and 840 nm. The loss-spectrum of these four channels is shown in Fig. 9.

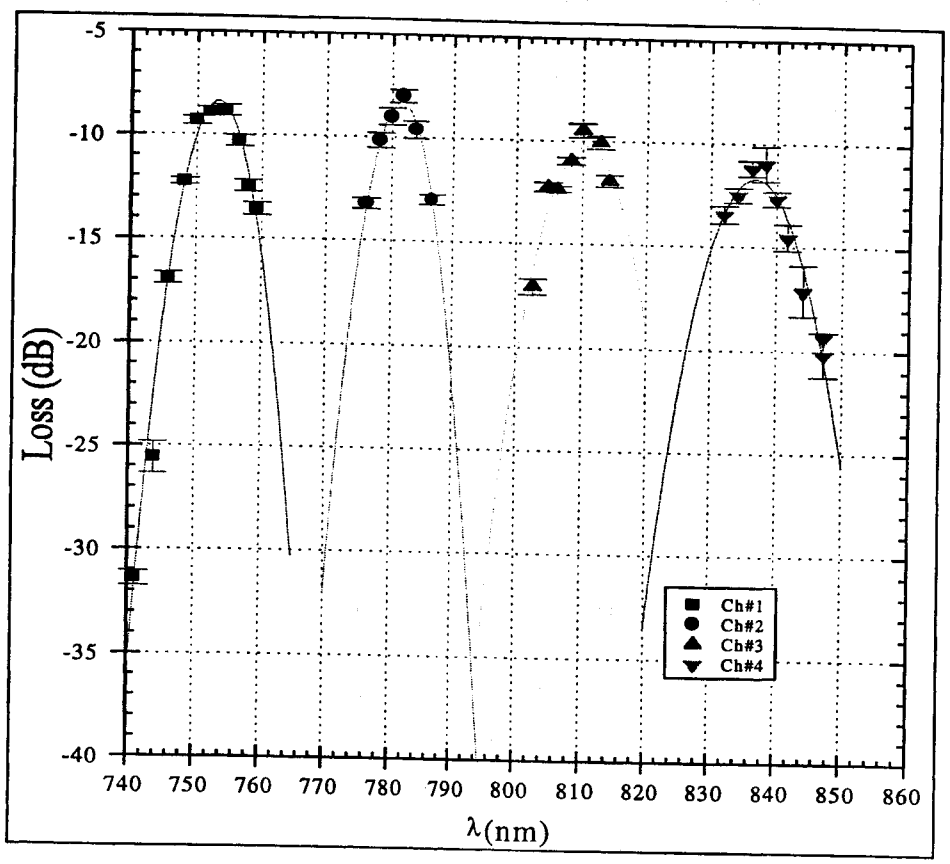


Fig. 9. Loss-spectrum of four channel WDDM for 750, 780, 810 and 840 nm.

This transmitter array gives us a realistic test of the problems encountered with real equipment when the wavelengths may not be exactly spaced at the desired $\Delta\lambda$ = 30nm, and when they are not at the desired values (750, 780, 810, and 840 nm). The output from the transmitter module was obtained from a single ST connector on the back panel of the module. This was transmitted into our prototype through a multimode fiber, connectorized with an ST/PC connector on one end, and pigtailed to a collimator on the other end. The collimator was acquired from OZ Optics, and produces a collimated beam of diameter of approximately 3mm. The initial hologram design was for a four-channel device, for wavelengths 750 nm, 780 nm, 810 nm, and 840 nm. For an output spacing of 250 μm, the required diffraction angle was calculated and a hologram was recorded for this design value. The collimator and hologram were mounted on a V-block on an optical stage. The diffracted beam from the hologram then travels to a mirror mounted on a mirror mount. After reflection from the mirror, the beam was focused by a lens, mounted on a simple post. This double convex, spherical, output coupling lens was chosen from several on hand, and had a focal length of 18mm. The fiber array chosen for this prototype has 4 multimode (50/125μm) fibers, mounted with separation of 250 μm in a silicon V groove, with each of the 4 fibers connectorized with ST/PC connectors. This output array was acquired from Wave Optics, Inc. Fig. 10 is a CCD camera picture of four WDDM spot separation using multiplexed thin film hologram.

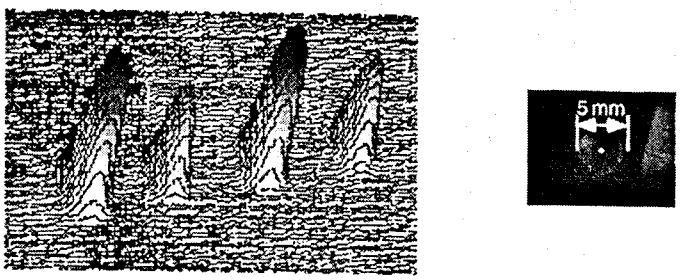


Fig. 10. WDDM spot separation using multiplexed hologram as observed through a CCD camera.

6. PARALLEL TRANSMISSION INTERFACE AND RELATED ISSUES

Here we assume that the future 3-D optical-memory devices will produce the data in a standard parallel channel format i.e. data streams in 8, 16, 32 or 64 –channel parallel outputs. The 8-channel parallel optical interface using WDM based architecture, conforming to HIPPI 6400-OPT standard can easily provide a data rate of 6.4 Gb/s[9] along with ample room for upgrading. In the sections below, we describe some of the issues and possible approaches to resolve them.

6.1 Optical Interface Architecture

One of the advantages of optical interconnections using a WDM based architecture is wider parallel signal transfer[15]. The WDM bit-parallel optical interface architecture can provide a better interface between high quality, high-speed optical signals and low speed electronic elements via parallelism. However, required throughput rate and interconnect lengths make the waveguide or fiber dispersion and resulting skew play important role in overall performance of the WDM based optical interconnects. An optical parallel interface has many advantages compared to its electronic counterpart. First, optical fibers and waveguides can carry high quality signal without excessive distortion at high pulse rate. Secondly, a parallel optical interface provides a compatible interface among a number of relatively low-speed electronic logic elements. Thirdly, high-quality optical pulses can reduce the holding time of electronic logic elements (setting time is the distinct bottleneck of the electronics).

The schematic of the basic architecture for our interconnect system is shown in Fig. 1. Here, the optical WDM bit-parallel interface will establish connection between a memory device and the processing unit. Fig. 11 shows the information flow between memory and processor via single optical fiber (in order to emphasize WDM multi-channel effects, many lines are used to represent virtual channels). A charge-coupled-device (CCD) is employed to read bytes from holographic memory and converted it to electrical signals. Its address is selected via a Memory Parallel Access Scheme and driven by a Device Driver. Data from memory is then feed into the WDM device using the Memory Access Scheme. At the receiver end (processor, for instance), data signals carried by multi-wavelengths are de-multiplexed into parallel bits, decoded, and finally provided to the application program interface for the processing unit and processed. While this unique architecture is of vital importance for high-performance interconnects and can be optimized for an optical/electrical interface, there exist several issues requiring investigation.

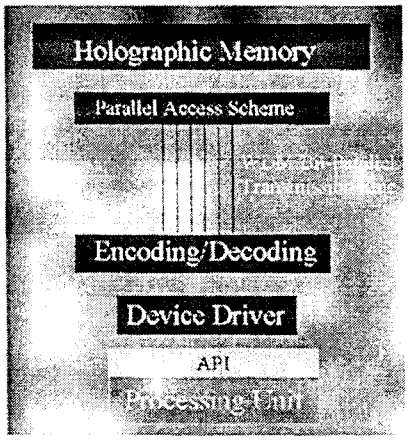


Fig. 11. Schematic of an interconnection between a memory device and processor.

- The multi-channel skew problem: Large channel-to-channel skew will limit the parallel pulse rate, which in turn determines the system performance.
- The parallel memory address problem: Ordinary computer systems are characterized by sequential processing capability. Especially, data retrieval is executed via serial data addressing and serial acquisition. A parallel memory address method is required to support parallel data transmission interface.
- The protocol issue: The protocol part of the interface determines how the information flows are coordinated. Protocol issue is an important issue in every communications network. HIPPI protocol is a very important standard for parallel interface. Optical bit-parallel protocol will heavily depend on HIPPI protocol, but will address its own protocol issue according to the features of the bit-parallel optical WDM scheme.
- Finally the hardware/software interface problem should be addressed.

6.2 WDM Optical Interface Protocol and Its Compatibility with HIPPI Protocol

Original HIPPI (high-performance-parallel interface) was designed for multiple electrical lines carrying parallel data. While each electrical line has limited bandwidth, multiple lines may provide a higher aggregated bandwidth. HIPPI-Serial specification was specified for fiber optical version of HIPPI, since original optical transmission used serial data format. HIPPI-6400-OPT specifies the 12-channel parallel point-to-point data transmission for up to 800 Mb/sec per channel data transmission[16,17]. A total of 12-bits are transmitted in parallel, where 8-bits are devoted to data transmission, 2-channels for control signal, and one-channel for frame signal to indicate start-stop position, and one channel for clock signal. In the 800 Mb/sec/channel transmission scheme, a HIPPI packet containing 32 data bytes and 8 control bytes requires 32 times parallel transmissions. It uses go-back-N protocol for re-transmission when there is a packet error. The error detection uses CRC checking. Its encoding scheme uses 4/5 code. It is small, simple and fast. HIPPI uses flow control to avoid congestion and uses a reservation mechanism to avoid buffer overflow. In the proposed scheme, the 12 virtual channels are realized by using a single fiber in conjunction with WDM technology. WDM optical interface protocol will resemble HIPPI parallel interface version, not the serial optical version.

HIPPI 6400 compared with other protocols[18,19]:

- **HIPPI-800:** provides low performance, has only flow control and no error control.
- **SCI :** has no error control and has limited flow control.
- **ATM:** has neither, is complex and prone to congestion.
- **Fiber Channel:** has both error and flow control, but not for all classes of service.
- **GHz Ethernet:** is like HIPPI-800 with small data-packets.

6.3 Software Management

Like other devices in a computer system, an optical memory device needs a device manager. Device drivers are part of the device manager used by an application process to call for an I/O operation such as a read/write operation. When the process makes a request to the device driver, the driver translates that request into controller-dependent commands and issues them to the device. After the device is put into operation, the driver either polls the controller to detect the completion of the operation or places information into a device status table entry to prepare for the device interrupt. Generally, hardware (device controller) controls the device, and software (device driver) controls the device controller.

Each operating system defines an architecture for its device management system [20]. These designs vary among systems, and there is no universal device driver software. Since device driver has many functions such as buffer manager as well as polling/interrupt, it is difficult to realize it in hardware, although hardware is always faster. High speed I/O is a demanding project for the high-speed optical communication. Regular I/O needs innovation in both techniques and new architecture.

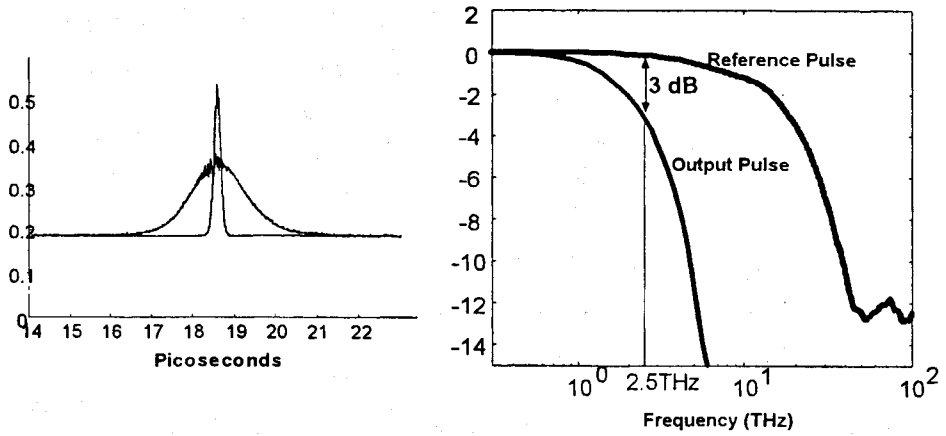
7. BANDWIDTH COVERAGE

Because of the parallel nature of the holographic storage systems, the fundamental data rate can be very fast. The effective data time is a measure of time required to fully retrieve an arbitrary data block from the system and is combination of the data transfer rate (the rate at which data are transferred from the memory to the user or CPU) and the data latency (the time lag between the address set-up and the appearance of data at the output). However, one of the most important parts of any holographic storage apparatus, the imager (CCD array or photodiode array) and imager to processor interconnect could be a determining factor for the data transfer time. The goal is to read out a 1-Mbit data page in 1 ms-100 μs time interval corresponding to a data rate of 1 - 10 Gb/s. Such a data rate is attainable only if signal can be read out from the CCD or photodiode arrays at a comparable rate. This can be facilitated by segmenting the two-dimensional array into blocks and read out these blocks of the CCD array in parallel with multiple output channels. Each block in this configuration is read in a serial manner. However, at such an aggregate data rate and relatively longer interconnection length, available bandwidth is a major concern for traditional interconnects. Interconnects based on light propagation in the polymeric waveguides and high performance multimode optical fiber can meet this challenge very effectively.

Waveguide structures for optical interconnect applications should have low optical losses at the wavelength of interest, and in order to achieve higher bandwidth the optical wavelength employed have to be in the shorter wavelength regime. Most favored optical wavelength at present are 850 and 980 nm because of the availability of VCSELs. However, optical loss is a major concern for low-power and efficient operation of polymer based waveguide devices. The challenge lies in the materials engineering to fine tune the properties of these polymers so that they retain desirable properties such as strength and temperature stability and provide low-loss optical propagation. To meet the required optical properties for low-loss

waveguide formation, and to ensure the desired electrical and mechanical properties imposed on Si CMOS processes, one approach could be to employ the polymers used in the electronic industries such as polyimides and BCBs for the waveguide fabrication. Cross-linked polyimides have excellent thermal stability (Tg >400 °C) and optical transparency.

Fig. 12(a) shows the pulse broadening of a 100 fsec optical pulse at 850 nm propagating through a 20.9 cm long polyimide waveguide. Fig. 12(b) shows the FTT results for the reference and the measured pulse output from the polyimide waveguide bus. It is clear from Figure 12(b) that a 2.5 THz (2,500 GHz) bandwidth is expected out of the optical interconnection system. Note that the waveguide dimension we are dealing with is in the highly multimode regime. The feasibility of using highly multimode waveguides as the optical paths greatly eases the process of patterning through microlithography.



(a) (b)

Fig.12 (a) Pulse Broadening of the 100 fsec optical pulse at 850 nm wavelength propagating through a 20.9 cm long polyimide waveguide, (b) Fast Fourier Transform (FTT) result showing the 2.5 THz base bandwidth of the polyimide-based optical waveguide

8. SUMMARY

We have introduced a novel approach to interface high-throughput 3-D optical memories to computer network using an optoelectronic interconnect based on WD(D)M technology (wavelength division (de)multiplexing) which can provide high speed and bi-directional transport of signals between the optical memory devices and processor boards. This interconnect will utilize polymer-based guided-wave devices in conjunction with multimode optical fiber/ fiber arrays and wavelength division (de)multiplexers (WD(D)M). This approach combines the advantages of WDM, polymer-based photonic devices, and state-of-the-art micro-fabrication techniques to make waveguide optical components and tapered channel waveguides to provide cost-effective, reliable, and low-loss propagation of optical signals and efficient input and output coupling among the arrays of optoelectronic devices and optical-fiber arrays. We have demonstrated a 4-channel WDDM device operating in the wavelength range 750-840 nm, and work to extend this to 12-channel is in progress. It has been shown that polymeric waveguide can provide band with in excess of 2.5 THz.

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