BI-DIRECTIONAL OPTICAL BACKPLANE BUS WITH MULTIPLE BUS LINES FOR HIGH PERFORMANCE BUS SYSTEMS

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1. INTRODUCTION

Over the past decade, the demand for more computing power has increased to such an extent that no single processor can provide the solutions in many applications. As a result, various efforts were made to build multiprocessor systems. Among those, systems based on electrical backplane buses, as shown in Fig. 1, have been prevailing in the commercial market mainly due to the ease of design and low cost. However, as the signal speed increases along the backplane, the transmission line effects become dominant, and the bus performance becomes limited by backplane physics[1,2]. Although advanced buses like Futurebus+[3] guarantee an incident wave switching, other inherent problems degrade the performance significantly[4]. As new faster processors arise, the electrical backplane buses can no longer supply the bandwidth required for high performance multiprocessor systems.

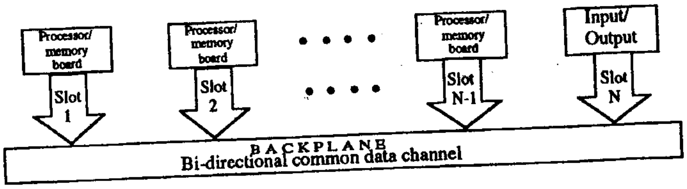

Fig. 1. Diagram of bus-based multiprocessor systems.

In an effort to increase the interconnection capacity, optics has been considered as an alternative for a long time[4]. Nonetheless, the burden of electrical-to-optical and optical-to-electrical conversions has prevented optics from growing as a viable solution. Recent development of efficient optoelectronic devices, especially in forms of arrays, has stimulated the research seeking for feasible optical solutions. In spite of these efforts, no general optical backplane compatible with existing electrical buses has been announced.

In order to provide a competitive optical solution, we developed a bi-directional optical backplane[5]. Unlike the previous optical backplanes aimed at special purpose computers[6], the backplane we reported is for general purpose, thus is compatible with standard multiprocessor backplane buses mentioned above. In this paper, we further developed a bi-directional optical backplane with multiple bus lines, which not only greatly increases the

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capacity of the backplane, but also is simple for transceiver design and easy for system packaging, so more feasible from practical point of view.

2. GENERAL PURPOSE BI-DIRECTIONAL OPTICAL BACKPLANE

Fig. 2 shows the schematic of the general purpose bi-directional optical backplane in a multiprocessor system which has nine processor/memory boards[5]. The signal from each board is coupled into and out of the backplane through a hologram acting as an input/output coupler, which is designed to provide a total-internal-reflected (TIR) beam within the waveguiding (glass) plate. An array of multiplexed holograms are recorded along each signal path for that purpose.

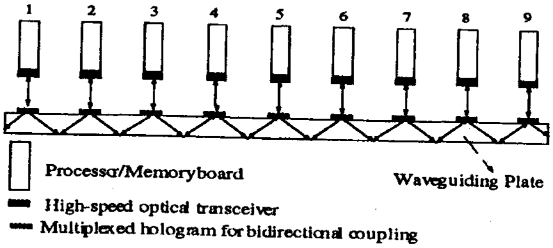

Fig. 2. Optical bi-directional backplane bus in a multiprocessor system with nine processor/memory boards.

A schematic illustrating the diffraction mechanisms associated with the multiplexed holograms is given in Fig. 3. In Fig. 3(a) $\vec{K}_1$ and $\vec{K}_2$ are grating vectors corresponding to the two gratings recorded inside the polymer film. Phase matching conditions for these two grating vectors are shown in Fig. 3(b). When the substrate-guided beam hits the multiplexed hologram with a Bragg angle, it is diffracted generating lights necessary for the bi-directional optical backplane, as shown in Fig. 3(c). The light diffracted surface-normally out of the backplane has the wavevector $\vec{k}'_{up}$, and is detected by the photodiode. The light with the wavevector $\vec{k}'$ provides power to the subsequent boards.

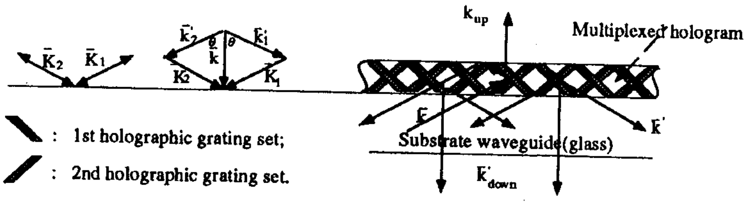

Fig. 3. Diffraction mechanism of light in by two sets of hologram gratings recorded on a glass substrate. (a). Two grating vectors recorded; (b). Light diffraction geometry by the gratings; (c).Light transmission, diffraction and reflection in side the bi-directional backplane bus.

3. HYBRID BACKPLANE WITH MULTIPLE BUS LINES

The optical bi-directional backplane we demonstrated above has only one bus line. For the architecture shown in Fig. 2, signal transmitting and receiving should have the same input/output window, which would introduce drawbacks in the wiring of the signal and packaging of the system. A different optical backplane scheme can easily overcome these difficulties by expanding the above backplane into multiple bus lines utilizing the $\vec{k}'_{down}$ beam as in Fig. 3(c). It incorporates arrays of transmitter and receiver multichip modules(MCM's) ıd easy for system

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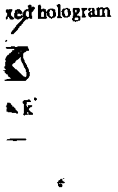

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on each side of the waveguiding channel as indicated in Fig. 4. This arrangement will result in a simpler transceiver design and ease the system packaging. Although we use the same waveguiding structure provided by the array of multiplexed holograms and the waveguiding plate, the overall design must be changed from Fig. 2 in order to be integrated with electrical processor/memory boards. Fig. 5 shows the overall structure of the proposed hybrid backplane. The center of one hologram is separated from those of the adjacent ones by 3 cm, which is the standard inter-board distance in electrical backplane environment.

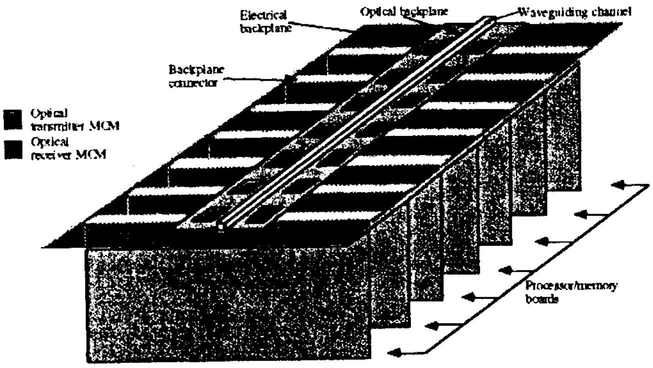


Fig. 4. Waveguiding structure for multichannel data path.

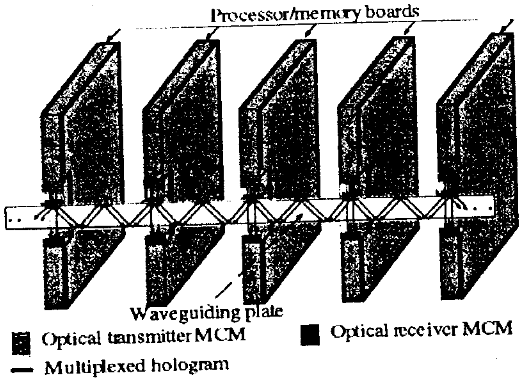


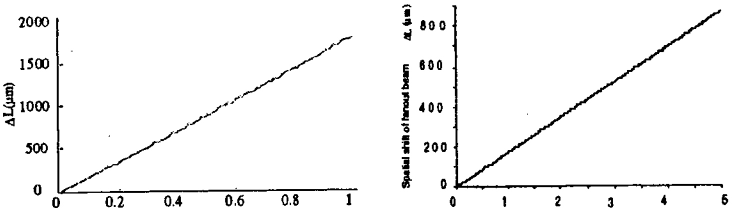
Fig. 5. Overall structure of the hybrid electrical/optical backplane.

There have been several different approaches[8,9] to utilize array devices in parallel data links. However, a number of recent attempts were stimulated by the advances of Vertical Cavity Surface Emitting Lasers(VCSEL's), which have evolved into efficient and reliable devices. VCSEL has many advantageous features for optical interconnection[10]. Some of those are small device size, low threshold current, small divergence angle, single longitudinal mode, and circular symmetric emission pattern. Yet another attractive feature of VCSEL technology is the capability of being fabricated into uniform, individually addressable, one and two dimensional arrays[11,12]. Many optical interconnection systems taking advantage of these VCSEL arrays have been developed[10,11,13]. Design issues using VCSEL arrays in free-space optical interconnects were addressed in the previous publication[14].

Fig. 6 shows the detailed diagram of waveguiding structure for an array of beams. It indicates the necessary components integrated into the transmitter and receiver multichip modules. As there is another set of fanouts directed to the transmitter modules, the optical isolators are inserted at the transmitter modules to block them. When the guided lights are packed closely with each other, crosstalk between the channels may degrade the performance of the system. A detailed effects of inter-channel crosstalk will be analyzed and simulated using arrays of lights.

from the input port, the minimum input power required is 2.7 μW, which can be easily achieved using state of the art VCSEL technology[16,17]. Take an average dynamic range of 30 dB, the input power range over which the receivers can perform properly without distortion and saturation lies between 2.7 μW-2.7 mW.

Among others, three major factors will affect the packaging of the backplane when integrated with transmitters and receivers on the processor/memory boards. These are: lateral misalignment, angular misalignment and wavelength instability. With self-aligned flip-flop solder bump bonding process[18], the lateral misalignment can be controlled with an accuracy of ~1 μm. Fig. 8 shows the lateral shift of the output signal beam with changes of input angular and wavelength variations after the signal travels through a distance of 3 cm along the backplane (thickness of 1 mm). Currently, the emission line width of VCSELs can be as narrow as less than 1 Å, so the misalignment due to this spectrum width factor can be ignored from Fig. 8(b). For a VCSEL with three quantum well (QW) InGaAs/GaAs active region, the lasing wavelength varies with temperature in a rate[19] of ~0.5 Å/K. To maintain a spatial shift within ±50 μm, the allowable temperature variation is ±5.8°K, which is in the limit of the contemporary electronic temperature stability control level[20]. However, from Fig. 8(a), the control of the angular alignment shouldn't be so easy a task. To keep the spatial shift of the output signal beam below an error range of ±50 μm (for a Silicon APD, typical size of active area is in the order of ~100 μm at 1 GHz), the angular misalignment should be within ± 0.03°. This stringent requirement is significantly relaxed by applying gradient index lens (GRIN), which is to be addressed in the following sections.



(a) (b)

Fig. 8. Lateral variation of the output signal beam with that of the (a) angular and (b) wavelength of the input beam.

Normally, the diameter of a photodetector is around 100 μm. For the VCSELs we will use in our lab, their light emitting window has a diameter of 15 μm and a lasing divergence angle of 5°. After propagating 3 cm in the bus, the spot size will become[21] 385 μm, which renders the detector impossible to respond in compare with the ~100 μm size of the detector active region for an 1 Gbit/sec system. So to make the system practical, a focusing collimating and focusing mechanism should be developed. As in Ref. 21, GRIN lenses will be used because of their miniature size and relatively easier in the packaging of the system than using microlenses. Most importantly, even for an angular misalignment of 2 degree, which will lead to an output spatial shift of ~3.6 mm in reference to Fig. 8(a), with the 0.25 pitch SLH type of GRIN lens[22] and at a wavelength of 0.85 μm, the beam shift is only ~50 μm. This will greatly ease the angular tolerance at the input port. Right now, the commercially available GRIN lenses have a minimum diameter of 1 mm, this determines that the input port separation on each MCM board should be larger than 1 mm compromise the above restriction and to reduce channel cross talk. At the detector port, the diameter of the GRIN lenses should be larger than that for the transmitter port to collect all the output energy and to tolerate the spatial shift induced by the misalignment of the input port.

5. CONCLUSIONS

We present the bi-directional optical backplane with multiple bus lines and discussed its application to a high-performance backplane bus for multiprocessor systems. Experimental

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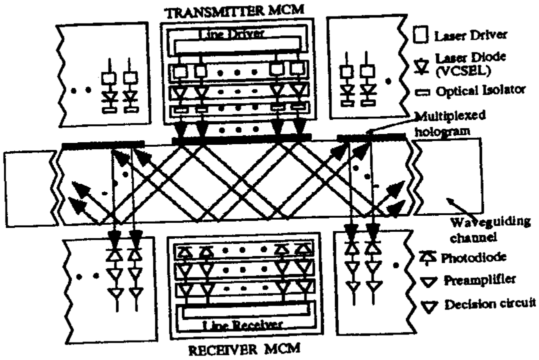

Fig. 6. Detailed diagram of waveguiding structure and transmitter and receiver modules.

4. EXPERIMENTS AND SYSTEM PERFORMANCE CONSIDERATIONS

Fig. 7 shows the Far field fanout patterns of the hybrid backplane bus with 2 bus lines operating at 850 nm which is the most popular wavelength for VCSELs. As for the backplane with a single bus line[5], a cascaded feature was also observed in the case of multiple bus lines.

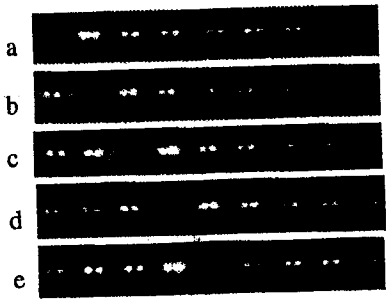

Fig. 7. Photographs with (a) the first, (b) the second, (c) the third, (d) the fourth and (e) the fifth channel sending optical signals to the other channels through the bi-directional optical backplane.

Power budget is another concern both for the system design and implementation. One of the major results from our previous theoretical calculation[5], aimed at minimizing fluctuations among all the output channels for the demonstrated case, is that the difference between the maximum and the minimum output intensity for different channels is about 17 dB. This is the optimized results and cannot be improved if considering the performance of all the output channels as a whole. For the detection of the optical signal, APD (avalanche photodiode) receivers are more suitable than PIN receivers for our system. This is because of their better sensitivity and higher input power dynamic range. Higher dynamic range can be obtained with APD receivers. For short wavelength (0.8-0.9 μm) detection, Silicon APD receivers are mostly used, and a dynamic range of about 40-50 dB has been obtained. In long wavelength (1.1-1.6 μm) region, Germanium and III-V alloys such as InGaAsP and GaAlAsSb give better performances, and a dynamic range of 25-40 dB has been reported[15]. The sensitivity of the receivers, that is, the minimum optical signal power required at the optical detector input for a desired receiver performance, determines the minimum power requirement of an optoelectronic system. For a bit error rate (BER) of 10^{-9}, operating at 500 Mbit/sec, having a multiplied primary dark current of 1000 nA, the sensitivity of Silicon APDs at 0.85 μm is around -45 dBm; for Germanium and InGaAs APDs, the sensitivities at 1.3 μm are about -41 dBm and -42 dBm, respectively[15]. All of the above sensitivities would result in a minimum signal power of around 0.04 μW at the input of the detectors. On considering the reflection results for backplane with two bus lines are demonstrated. Power budget consideration is discussed based on the previous theoretical results and an input power range of 2.7 μW-2.7 mW is found to ensure the normal operation of the bus with nine processor/memory boards. Finally, a GRIN lens focusing mechanism is introduced into the hybrid system. It is found that not only can the GRIN lens carry out the functions of collimating and focusing signal beams, but also ease the alignment of the input channels.

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