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Polygonal Gratings for Wafer Scale 1-to-many Optical Clock Signal Distribution

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Abstract

In contrast to volume holographic material where 1-to-many fanouts are realized using multiplexed volume holograms, we report in this paper the first Si-based surface relief polygonal gratings aiming at optical clock signal distribution application. Surface relief grating with 1μm period (0.5μm feature size) was fabricated using reactive ion beam etch (RIE). Both hexagonal and square gratings were demonstrated for 1-to-4 and 1-to-6 fanouts. Surface-normal input and output coupling schemes were carried out with efficiency as high as 65%. Employment of substrate modes in silicon instead of the guided modes greatly releases the required grating spacing for the demonstrated two-way surface-normal coupling. Clock signal distribution operating at 1.3μm with 7.5 GHz clock speed was demonstrated with signal to noise ratio as high as 60 dB.

With the advent of higher clock speeds and distributed multiprocessor computer architectures, a great deal of interest has arisen in synchronously distributing a clock signal over all the processors in a computer with an acceptable clock skew[1]. Unfortunately, at the clock speeds above 500 MHz, a synchronous global clock distribution system is very difficult to attain using electrical interconnects due to the skin-effect induced losses, impedance-mismatch due to large fanouts, and RLC-related charging times which are detrimental for the realization of such an electrically interconnected high speed system. Because of the high bandwidth inherent in optical signals, various guided wave optical clock distribution schemes have been investigated to alleviate such a problem. Photopolymer-based multiplexed volume holograms[2] have been employed to achieve massive fanouts up to 59/nodes[3]. Surface relief materials have also been utilized by using different diffraction orders of surface relief gratings working in a reflection mode[4] to achieve the required fanout. Due to the nature of non-multiplexibility, the surface relief grating is primarily employed as a 1-to-1 interconnect device with relatively low interconnectivity{5]. For 1-to-many fanout optical interconnects employing surface relief material with a single fanout node, new device configuration is needed to solve this problem.

In this paper, we demonstrate the first Si-based polygonal gratings for 1-to-many fanouts. A linear grating is converted into a polygonal format with a required grating vector for each predestined fanout direction. A central polygonal input coupling grating and surrounding linear output coupling gratings are employed to provide the desired optical clock signal distribution. As shown in figure 1, equivalent optical paths and thus minimized clock skew are provided through this approach. A double-side polished Si wafer is used to minimize the surface scattering losses as the signal travels through the bulk of the Si wafer. The number of fanout is determined by the total facets associated with the polygonal grating needed to realize the 1-to-many clock signal distribution. The basic coupling configuration is illustrated in the inset of Fig.1. In order to provide a substrate guided wave with a bouncing angle Θ_t within the silicon substrate from the surface normal incident direction, the grating period Λ has to satisfy the following equation, i.e.,

$$\Lambda = \frac{\lambda}{n_{Si} \bullet \sin\Theta_t} \tag{1}$$

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where n_{Si} is the refractive index of silicon, and λ the wavelength of operation. For an operating wavelength of 1.3μm with air as the cladding medium, the critical angle for total internal reflection is less than 20° which makes a grating period of 1μm applicable for this application. Note that the zig-zag bouncing mode described in this paper is the substrate guided waves which were defined as "substrate modes" in the conventional terminology of integrated optics[6]. Employment of these modes significantly releases the grating spacing requirement for surface-normal coupling and therefore facilitates the fabrication process. Both the central polygonal and linear output gratings have a period of 1 μm, allowing light to be efficiently coupled into and out of the Si wafer substrate guided modes in the surface normal direction. The other major advantage of the substrate guided wave approach is that, since the gratings can be written onto the Si surface using optical lithography followed reactive ion etching, an array of grating shapes and depths can be selected to optimize the diffraction efficiency. The 1-to-many fanout interconnects presented herein also significantly reduce the optical power requirements. This is because the relatively low loss of the Si substrate at the wavelength of operation, i.e., 1.3 μm when compared with such conventional guided wave devices as Si_xGe_{1-x}/Si, $Si/SiO_2/Si$ where typical waveguide losses are in the region of 0.1 to 1.0 dB/cm . Employment of a Silicon substrate as the grating medium also allows for greater temperature dynamic range in system packaging due to the same thermal expansion coefficient as that of Si-based VLSI chips.

In this paper, 1-to-4 and 1-to-6 fanouts were demonstrated. The mask patterns were generated using Auto CAD and additional software written specifically for this application. Photoresist pattern was used as the masking material for the etch process. The first stage of the RIE process was the removal of SiO_2 layer using CF_4 gas and the second stage is the formation of the grating microstructure using RIE with Cl_2 and He as the active gasses with flow rates of 30.0 cm^3/sec and 94.2 cm^3/sec, respectively. This fabrication process results in a rectangular grating profile whose depth can be controlled through the control of RIE etch parameters. Figure 2 shows an SEM photograph of a typical grating profile attained with this technique. In using this technique with 1 μm period gratings, careful process control must be used to insure that the photoresist is removed all the way down to the wafer in the exposed stripes of the grating.

To characterize etch rate of RIE samples, diffraction efficiencies of grating samples were measured as a function of etch time for three different wavelengths: 0.632, 1.06, and 1.32 μm in reflection mode. This was done in order to determine the actual depth of the fabricated gratings. An accurate evaluation of the grating depth at various etch times can be determined using multiple wavelength approach[7,8]. The measured data of etch depth as a function of etch time with other parameters fixed is summarized in figure 3. Based on the etch rate data depicted in figure 3, 1-to-4 and 1-to-6 fanout gratings were successfully fabricated using RIE. As we mentioned earlier that the employment of Si substrate modes as the signal carrier beams significantly reduces the spatial resolution requirement of the microlithography. With an operating wavelength at 1.3μm, the grating with 1μm period will be sufficient to provide the required TIR beams within Silicon substrate for the proposed optical clock signal distribution. The microstructure of the fabricated 1-to-4 square grating and the 1-to-6 hexagonal grating are further illustrated in figures 4(a) and 4(b) where equal partitions of the real estate of the grating is clearly indicated. 1-to-4 and 1-to-6 fanouts were realized using these devices which converts surface-normal incident beams to substrate guided waves with a bouncing angle of 21.6°. A 1.3 μm Nd:YAG laser with a circularly polarized beam is focused onto the center polygonal grating of the device. Figure 4(c) is an infrared photograph of a 1-to-4 fanout device in operation. The beam propagation direction is clearly explained by viewing figure 1. Both input and output beams are coupled surface-normally. Such a device configuration is compatible with the implementation of surface-normal transmitters and receivers such as vertical cavity surface emitting lasers.

The optical clock signal is generated using an HP 8703A lightwave component analyzer and detected using an Epitaxx ETX-25B high speed InGaAs PIN-photodiode. This particular prototype device was fabricated in a single lithography step followed by an RIE step with the etch time set to produce a grating depth of 0.3 μm, optimizing the coupling efficiency into the substrate. For this case, 65% of the light incident on the polygonal grating is coupled into the substrate. Of the remaining 35%,

25% of the incident power was in the zeroth order reflected mode and 10% was transmitted through the device. In this prototype, each of the beams from the four nearest output coupling gratings can be readily observed which coupled the optical wave surface-normally as indicated in Figure 1.

The modulated 1.3 μm laser beam is collimated and then coupled surface-normally into the 1-to-4 surface-normal fanout grating shown in Fig.4(a). This Si-based grating device converts the surface-normal in-coming beam into four substrate guided waves which are governed by the total internal reflection (TIR) effect. The four substrate guided waves were coupled out surface-normally through four separate output grating couplers shown in the four corners of the fanout device shown in Figure 4(c). The detected signal at the output was analyzed using a sampling scope and a microwave spectrum analyzer. The measured 7.5 GHz clock speed shown in the analyzer is further illustrated in Fig.5. To understand the bandwidth coverage of the optical clock singal distribution system, we further measured the frequency response of the photodiode. The result concluded that the 7.5 GHz was due to bandwidth of the photodiode rather than the optical clock signal distribution system itself. Our data show that we are limited by the bandwidth of the photodiode employed for this experiment. It is clear to us that the optical clock signal distribution system shall have a bandwidth coverage much larger than that of the graph shown in Fig.5. The demonstration shown herein has an interconnection distance of 4 cm with a clock speed of 7.5 GHz.

In conclusion, we have demonstrated a novel architecture for optical clock signal distribution. Employment of substrate modes instead of conventional guided modes as the signal carrier significantly releases the grating spacing for the required phase-matching condition. Surface relief gratings with multiple grating vectors were fabricated using square and hexagonal patterns. 1-to-4 and 1-to-6 fanouts with uniform intensities were demonstrated at 1.3 μm. Using this method, a prototype device with an input/output coupling efficiency of 65% having a measured 7.5 GHz clock speed with interconnection distance of 4 cm were demonstrated.

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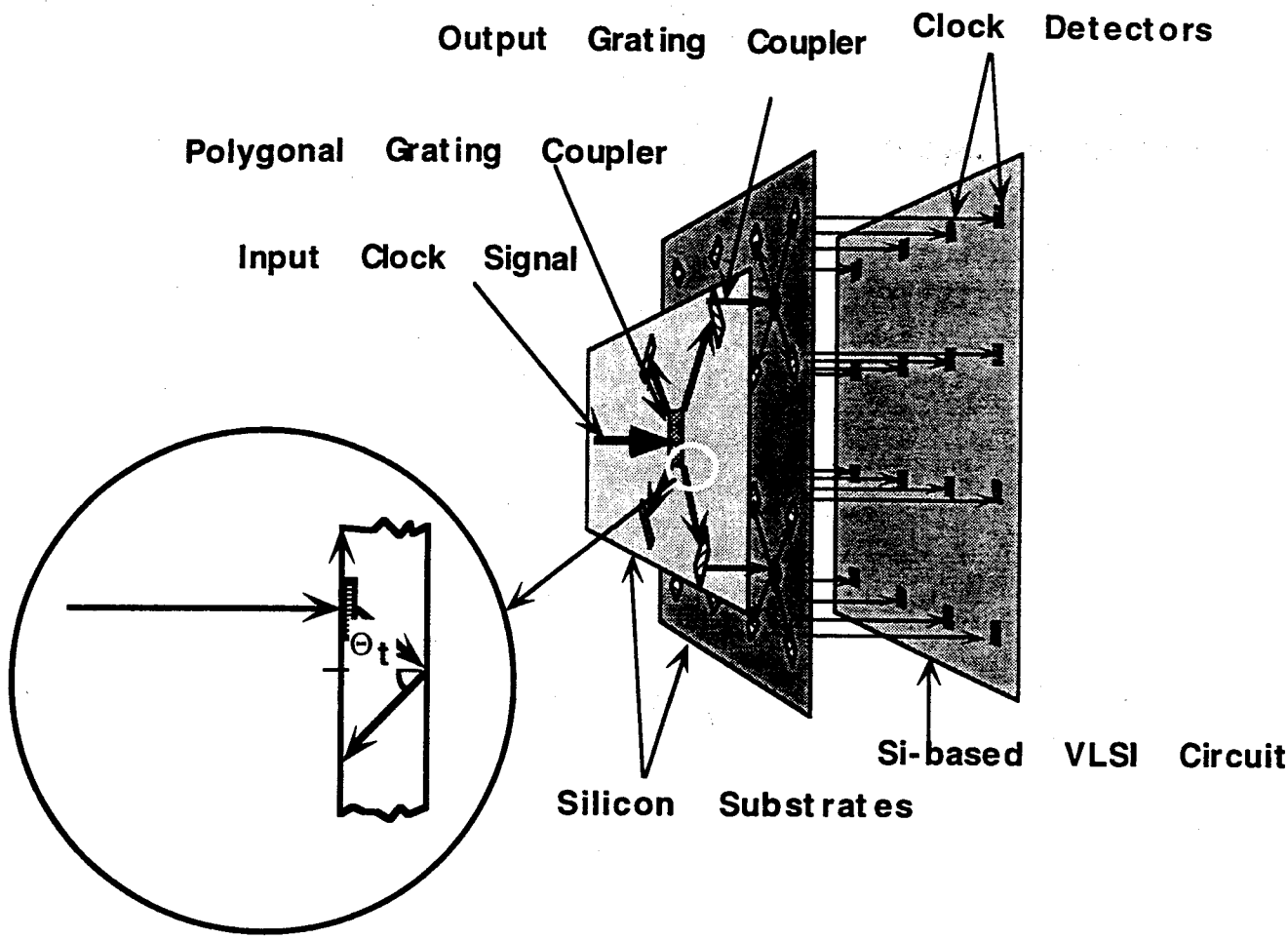
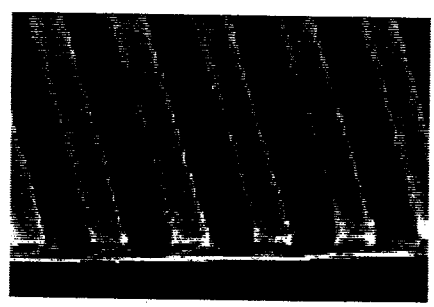


Figure 1: Schematic of Si wafer based optical clock distribution system. The High Speed clock signal is input onto the center grating via an optical fiber and laser . It is then distributed to the elements of the multi chip module via an array of surface relief gratings.



0.5 μm Feature Size

Figure 2: Scanning electron microscope picture of a grating after with 1mm feature size 120 second etch time. The approximate etch depth is 0.5 μm.

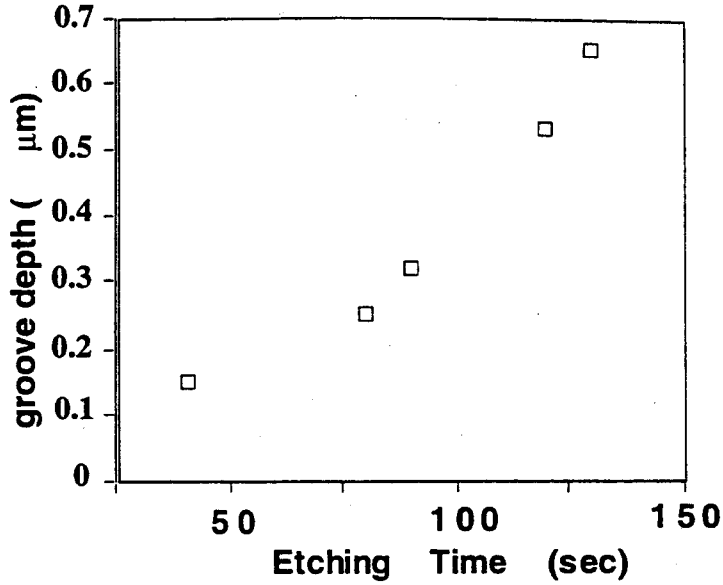
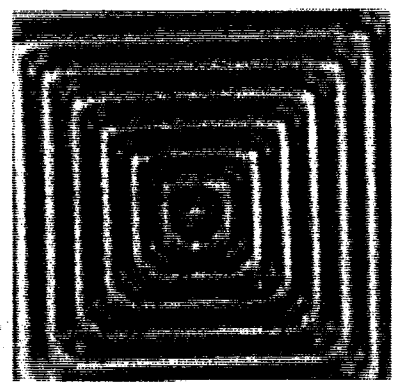
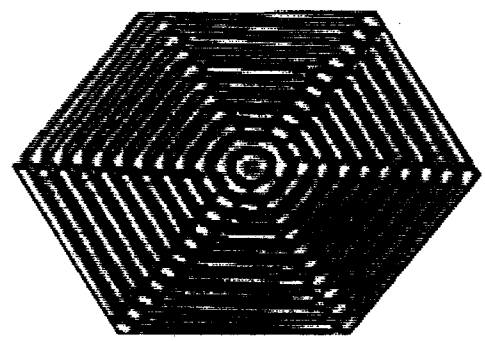


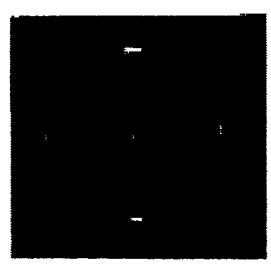
Figure 3: Etch Rate of Reactive Ion Etching (RIE) on Silicon using Cl_2 and He as the active gasses with flow rates of 30.0 cm^3/sec and 94.2 cm^3/sec, respectively.



(a)



(b)



4(c)

Figure 4a: Microscope photograph of the input coupling hexagonal 1-to-6 fanout grating structure with 1mm feature size in silicon used to create a 1 to 6 fanout in the substrate. 4b: 1μm period square 1-to-4 grating structure used to create the 1 to 4 fanouts. 4(c) Demonstration of 1-to-4 Surface-normal Fanout using a Square Input Grating and Four Output Linear Gratings

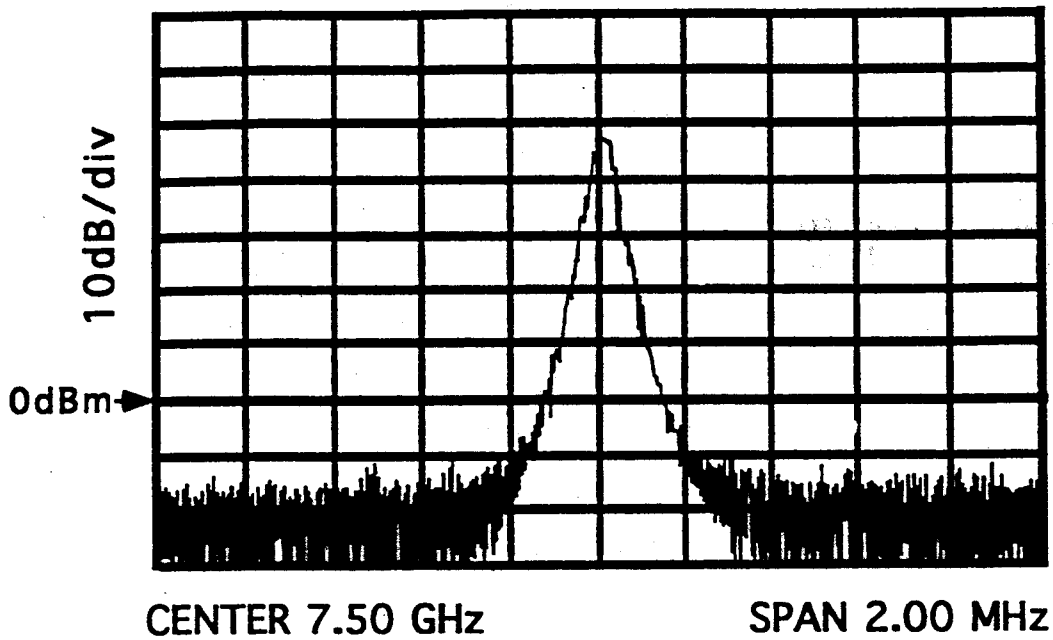


Figure 5 **The Clock Signal Distribution System Based on Si Substrate Guided Wave, 7.5 GHz Clock Signal Detected**