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Optoelectronic interconnect architecture of parallel modified signed-digit adder and subtracter

Degui Sun*, Naxin Wang†, Liming He†, Zhaoheng Weng†, Daheng Wang†, and Ray T. Chen*

*Microelectronics Research Center
Department of Electrical and Computer Engineering
The University of Texas at Austin, TX 78712, USA

†Changchun Institute of Optics and Fine Mechanics
Academia Sinica
Changchun 130022, P. R. China

ABSTRACT

In this paper, a space-position-logic-encoding scheme is proposed, which not only makes best use of the convenience of binary logic operation, but is also suitable for the trinary property of modified signed-digit numbers. Based on the space-position-logic-encoding scheme, a fully parallel modified signed-digit adder and subtracter is built by use of optoelectronic switch and microstructure interconnect technologies. Thus an effective combination of a parallel algorithm and a parallel architecture is implemented. Finally, both simulation results and experimental results are provided.

1. INTRODUCTION

There are two options to develop parallel digital optical computing systems: one is to research the carry-free or carry-limited parallel algorithm, the other is to research the optical implementing architecture. Of course, the best selection is an effective combination of these two options. The modified signed-digit (MSD) algorithm is an effective carry-free or carry-limited algorithm, and symbolic substitution is an optical parallel implementing approach; thus an optical MSD parallel computing system based on symbolic substitution is a typical example of a combination of a parallel algorithm and a parallel implementing approach[1-5]. In fact, the important factor of the realization of the conversion from algorithm to the hardware is having an effective encoding scheme. However, in the parallel optical computing systems, in terms of the proposed optical pattern encoding and optical polarization encoding for symbolic substitution, the space size taken by each operand bit cannot be made very small, which limits the miniaturization and integration of MSD optical computing systems. In addition, both substitution rules and optical approaches for implementing the rules are generally difficult, which limits the further development of multibit parallel MSD optical computing systems. Multi-dimensional optical interconnection is another important parallel implementing approach in digital optical computing which can help the switches to complete logic operations as well as implementing data transportation and switching. In digital optical computing, perfect shuffle, crossover, and butterfly are three typical regular interconnect networks[6-8]. Butterfly, especially, has been verified to be the most suitable for optical implementation[9]. The purpose of this paper is to discuss implementation based on the effective combination of the MSD algorithm and the butterfly interconnection architecture by use of a space-position-logic-encoding (SPLE) scheme, which exploits both the carry-free property of the MSD algorithm and the convenience of binary logic operation with optoelectronic logic technology. Finally a 3-bit experimental model of parallel adder and subtracter based on MSD algorithm and finer interconnect technology is built and correct experimental results are provided.

2. MSD ALGORITHM REVIEW

An MSD number can be written as

$$D_{MSD} = [1, 0, \bar{1}] \quad (1)$$

where $\bar{1}$ represents -1 . Then each decimal number can be represented in the MSD number system by the coefficients of the polynomial:

$$D_{10} = [1, 0, \bar{1}]2^{n-1} + \dots + [1, 0, \bar{1}]2^i + \dots + [1, 0, \bar{1}]2^0 \quad (2)$$

For two MSD numbers, $X_{MSD} (= X_{n-1}, \dots, X_i, \dots, X_0)$ and $Y_{MSD} (= Y_{n-1}, \dots, Y_i, \dots, Y_0)$, the addition can be performed through a three-step operation[1,2]. At the first step, a weight digit W_i and a transfer digit T_{i+1} are produced by Eq.(3):

$$X_i + Y_i = 2T_{i+1} + W_i, \quad (3)$$

where all the values of T_{i+1} and W_i are determined by their truth-tables as shown as Fig.1(a) and Fig.1(b), respectively.

T		
1	1	0
0	1	$\bar{1}$
$\bar{1}$	0	$\bar{1}$
	1	0
	0	$\bar{1}$
	(a)	

W		
1	0	0
0	$\bar{1}$	1
$\bar{1}$	0	0
	1	0
	0	$\bar{1}$
	(b)	

Fig. 1. Truth tables of the first-step operation of MSD addition: (a) for transfer digits T , (b) for weight digits W .

At the second step, another pair of weight digit W'_i and transfer digit T'_{i+1} are produced by Eq.(4):

$$W_i + T_i = 2T'_{i+1} + W'_i, \quad (4)$$

where all the values of T'_{i+1} and W'_i are determined by their truth-tables as shown in Fig.2(a) and Fig.2(b), respectively.

T'		
1	1	0
0	0	0
$\bar{1}$	0	$\bar{1}$
	1	0
	0	$\bar{1}$
	(a)	

W'		
1	0	0
0	1	$\bar{1}$
$\bar{1}$	0	0
	1	0
	0	$\bar{1}$
	(b)	

Fig. 2. Truth tables of the second-step operation of MSD addition: (a) for transfer digits T' , (b) for weight digits W' .

The third step generates the final sum digit S_i :

$$S_i = W'_i + T'_i, \quad (5)$$

		S(=T)		
1		1	1	0
0		1	0	1
i		0	1	1
		1	0	1

Fig. 3. Truth tables of the third-step operation of MSD addition: for the final sum S .

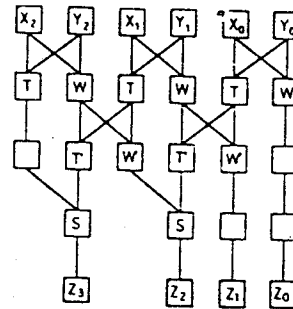


Fig. 4. Butterfly architecture implementing 3-bit MSD addition and subtraction.

where all the values of S_i are given by the truth-table as shown in Fig. 3, which is the same as Fig. 1(a). In terms of the three step operations of MSD addition, the MSD addition of two 3-bit digits can be depicted in the butterfly interconnection architecture as shown in Fig. 4, where $X(= X_2X_1X_0)$ and $Y(= Y_2Y_1Y_0)$ are augend and addend, respectively, and $Z(= Z_3Z_2Z_1Z_0)$ is the final addition result.

3. SPACE-POSITION-LOGIC-ENCODING SCHEME

As described above, the difference between MSD digit and binary digit is that binary digit has only the two digits of 1 and 0, while MSD digit has the three digits of 1, 0, and $\bar{1}$, respectively. Therefore, it does not like the binary digit to take higher and lower voltages as an encoding scheme. In digital optical computing, because of optical property and the symbolic substitution theorem, pattern encoding, polarization encoding[2-4], and other encoding schemes[10] occur successively. In this section we propose a space-position-logic-encoding (SPLE) scheme as shown in Fig. 5, in which three different space positions, A, B, and C (or a, b, and c), are used to represent 1, 0, and $\bar{1}$ of MSD digits in which three light-emitting diodes (LEDs) or laser diodes (LDs) at A, B, and C (or a, b, and c) represent only one MSD bit; namely, only one LED or LD has a light signal, and a light signal at a different position of the i th bit represents a different value. For example, the light signal of the LED or the LD at position A of the X_i bit represents $X_i=1$, and at the same time, the LEDs or LDs at positions B and C of the X_i bit have no light signals; the light signal of the LED or the LD at position B of X_i bit represents $X_i=0$, and at the same time, the LEDs or the LDs at position A and C of the X_i bit have no light signals; the light signal of the LED or the LD at position C of X_i bit represents $X_i=\bar{1}$, and at the same time, the LED or the LD at positions A and B of the X_i bit have no light signals. Thus each space position has two states, either having a light signal or having no light signal, which is similar to the logic operations of the binary algorithm. Therefore we call the encoding scheme a space-position-logic-encoding (SPLE) scheme. Then with the SPLE scheme the truth-tables for the three operations of MSD additions as shown in Figs. 1, 2, and 3 become the new forms as shown in Figs. 6, 7, and 8, where any table has nine states, i.e., the nine combinations of the three digits (A, B, and C) of augend X_i and the three digits (a, b, and c) of addend Y_i . The three digits of augend are arranged in a column and three digits of addend are arranged in a row, as shown in Figs. 6, 7, and 8. Of course, each state is an AND result of two digits.

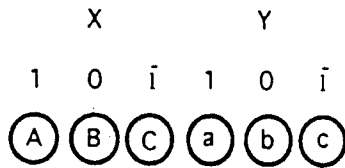


Fig. 5. Space-position-logic-encoding (SPLE) scheme in which three space position codes, A, B, and C (or a, b, and c), stand for 1, 0, and $\bar{1}$.

	T		
A	a	a	b
B	a	b	c
C	b	c	c
	a	b	c

(a)

	W		
A	B	C	B
B	C	B	A
C	B	A	B
	a	b	c

(b)

Fig. 6. Truth tables of the first-step operation of MSD addition represented by the SPLE scheme: (a) for transfer digits T , (b) for weight digits W .

	T'		
A	a	b	b
B	b	b	b
C	b	b	c
	a	b	c

(a)

	W'		
A	B	A	B
B	A	B	C
C	B	C	B
	a	b	c

(b)

Fig. 7. Truth tables of the second-step operation of MSD addition represented by the SPLE scheme: (a) for transfer digits T' , (b) for weight digits W' .

A	G_1	G_2	G_3
B	G_4	G_5	G_6
C	G_7	G_8	G_9
	a	b	c

Fig. 8. Truth tables of the third-step operation of MSD addition represented by the SPLE scheme for the final sum S .

	S(-T)		
A	a	a	b
B	a	b	c
C	b	c	c
	a	b	c

Fig. 9. Unitary detecting array, where G_1, G_2, \dots, G_9 are nine detecting elements.

4. BUTTERFLY INTERCONNECT ARCHITECTURE

In terms of all the truth tables of MSD addition expressed in the SPLE scheme, any table has nine states, and each state is an AND result of two digits from a row and a column, respectively. Thus we can use a unitary switch module including nine detecting elements to stand for all the truth tables of MSD addition, as shown in Fig. 9, in which all the detecting elements (G_1, \dots, G_9) can be used for the nine states of any truth table. It can be noted that G_1 is the detecting element for the AND operation of A and a, G_2 is the detecting element for the AND operation of A and b, and so forth, until G_9 is the detecting element for the AND operation of C and c. To build a multilayer butterfly interconnection architecture corresponding to the multibit computing, we use the most basic butterfly to represent the nine AND operations (Fig. 9) of augend

digits (A, B, and C) and addend digits (a, b, and c) as shown in Fig. 10. It can be noted with ease that the nine combinations come from 11 pairwise combinations of 12 operand digits (double A, B, C and a, b, c). This butterfly interconnect architecture is the easiest because all the interconnection operations are performed between two adjacent nodes, and it is especially suitable for the microstructures such as grating and waveguide.

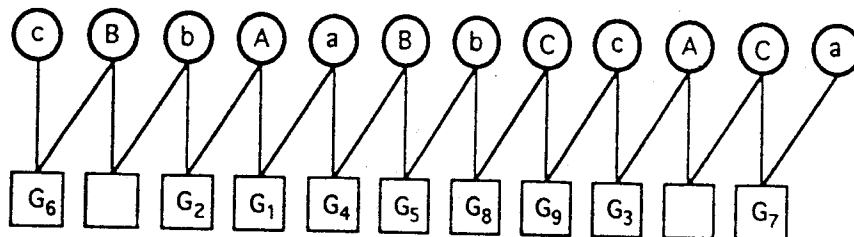


Fig. 10. Corresponding architecture of operands (A, B, and C; a, b, and c) represented by the simplest butterfly interconnection.

The AND results from the nine detecting elements on the detecting planes of modules can drive several LEDs or LDs on the light-emitting planes, which give light signals for the next operations. The arrangement of all the possible light signals (A, B, and C; a, b, and c) on the light-emitting planes of modules is the same as that in Fig. 10, but only the detecting elements receiving two light signals can perform AND operations and make their LEDs or LDs produce light signals at the corresponding positions. Figures 11(a), 11(b), and 11(c) represent the operating examples of $X_i=1$ and $Y_i=0$, $W_i=1$ and $T_i=0$, and $W_i=1$ and $T_i=0$, respectively. Obviously each MSD bit addition is completed through three stages of the simplest butterfly interconnections and three operations, as shown in Fig. 11, where hatched circles indicate having light signals and hollow circles indicate having no light signals. For the first stage of operations, as shown in Fig. 11(a), if $X_i=1$ and $Y_i=0$, i.e., A_i and b_i have light signals, then only the detecting element G_2 can receive two light signals and perform AND operations and can drive its next-stage LED's or LD's a of T_{i+1} and C of W_i for the next stage of operations according to Figs. 6(a) and 6(b), respectively. For the second stage of operations, as shown in Fig. 11(b), if $W_i=1$ and $T_i=0$, i.e., A_i and b_i have light signals, then only the detecting element G_2 can receive two light signals and perform AND operations and can drive its next-stage LED's or LD's b of T_{i+1} and A of W_i for the next stage of operations according to Figs. 7(a) and 7(b), respectively. For the third stage of operations, as shown in Fig. 11(c), if $W_i=1$ and $T_i=0$, i.e., A_i and b_i have light signals, then only the detecting element G_2 can receive two light signals and perform AND operations and can drive its next-stage LED's or LD's a of S_i of the i th bit according to Fig. 8. The interconnections among all the operand bits can be performed according to the standard butterfly structure as shown in Fig. 4, which can be implemented by use of electrical interconnection within the switch modules. The interconnections among the 12 digits of two groups of operand digits can be completed by use of optical interconnection. Therefore with the SPLE scheme and the simplest butterfly interconnections a fully parallel MSD adder can be constructed by use of three stages of optical butterfly interconnection and four switch modules, M_0 , M_1 , M_2 , and M_3 , which can complete logic operations and signal arrangements, as shown in Fig. 12. With the SPLE scheme, the MSD subtraction can also be performed as MSD addition by use of the complement of the subtrahend, i.e., with 1 as $\bar{1}$, $\bar{1}$ as 1, and 0 as 0 in the subtrahend. Therefore the MSD architecture in this paper is really a parallel optoelectronic MSD adder and subtracter.

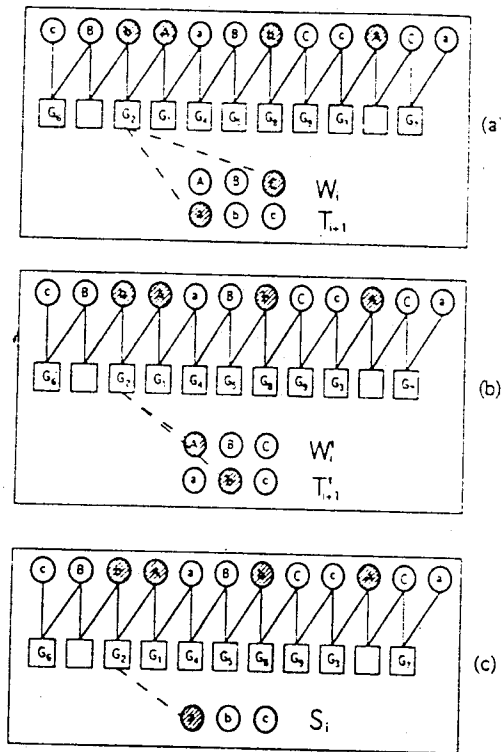


Fig. 11. Operation examples of an MSD adder and subtracter: (a) $X_i = 1, Y_i = 0$; (b) $W_i = 1, T_i = 0$; (c) $W_i = 1, T_i = 0$. Hatched circles indicate having light signals, and hollow circles indicate having no light signals.

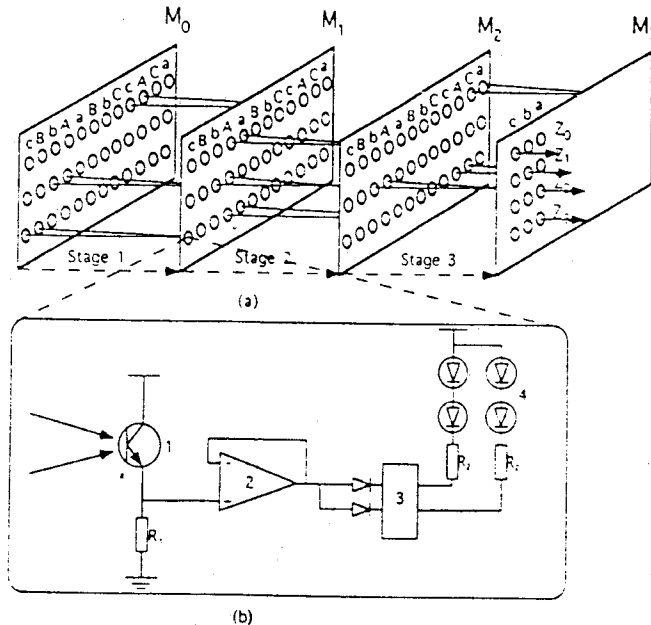


Fig. 12. Architecture of an optoelectronic MSD adder and subtracter: four switch modules and three stages of the simplest butterfly interconnection. (a) construction; (b) the circuit of a switch cell. 1 photo-diode; 2 modifier; 3 electronic gate device; and 4 LEDs.

5. EXPERIMENTS

With optoelectronic and fiber interconnect technologies, an experimental model of 3-bit optoelectronic parallel MSD adder and subtractor has been built by us as shown in Fig. 13, and the correct experimental results have been obtained.

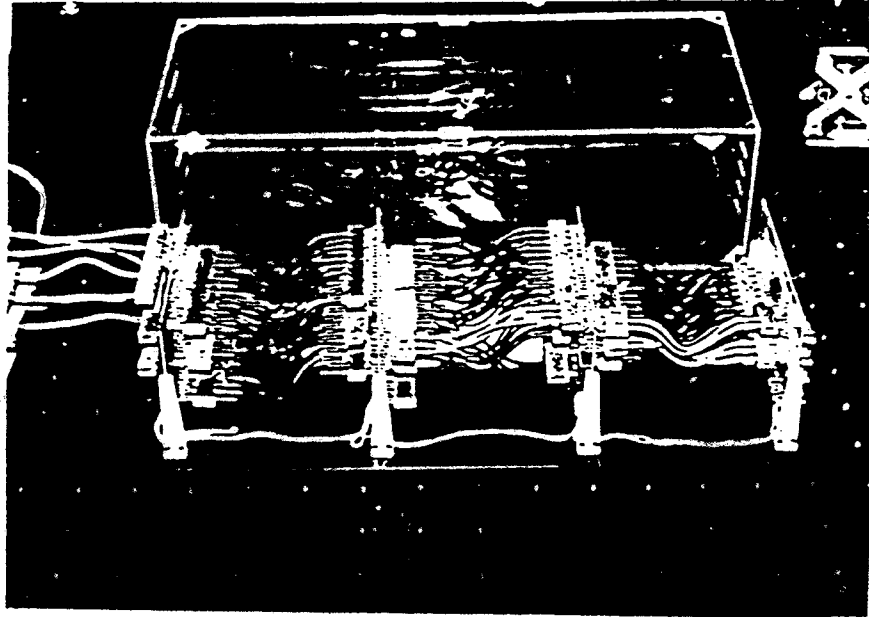


Fig. 13. Experimental model of 3-bit MSD adder and subtractor by use of optoelectronic logic and fiber interconnection technologies.

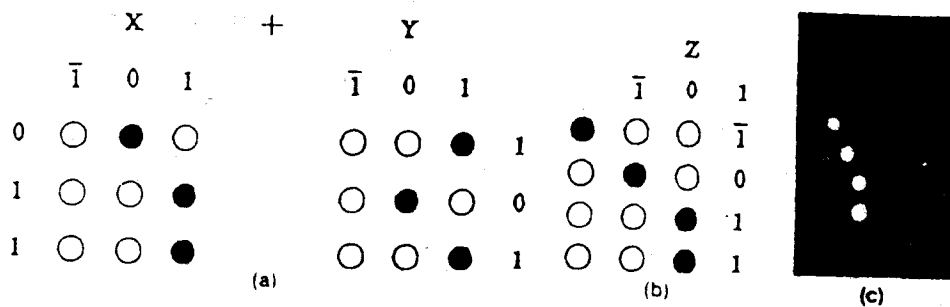


Fig. 14. Simulation and experimental results of an MSD addition $(6)_{10} + (5)_{10} = (110)_{MSD} + (101)_{MSD}$

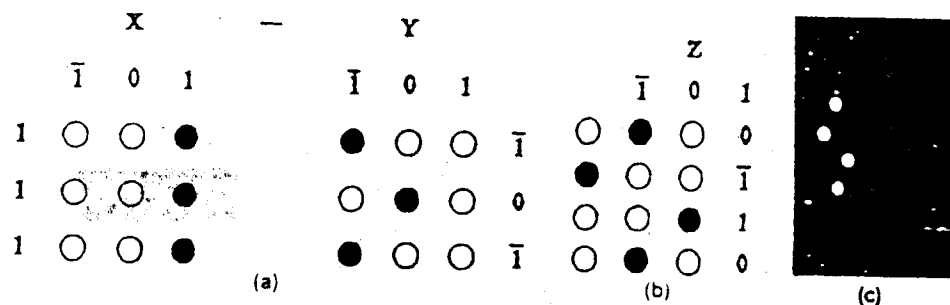


Fig. 15. Simulation and experimental results of an MSD subtraction $(7)_{10} - (5)_{10} = (111)_{MSD} + (\bar{1}0\bar{1})_{MSD}$

For example, for the addition of 6 and 5, $(6)_{10} + (5)_{10} = (11)_{10}$ can also be written as $(110)_{MSD} + (101)_{MSD}$; the simulation input signals, the simulation addition results, and their experimental results are obtained as shown in Fig. 14(a), 14(b), and 14(c), respectively, where filled circles indicate having light signals and hollow circles indicate having no light signals. It can be noted from Figs. 14(b) and 14(c) that both simulation and experimental results are $(110\bar{1})_{MSD} = (11)_{10}$, which are obviously correct. For the subtraction of 7 and 5, $(7)_{10} - (5)_{10} = (2)_{10}$ can also be written as $(111)_{MSD} + (\bar{1}0\bar{1})_{MSD}$; the simulation input signals, the simulation subtraction results, and their experimental results are obtained as shown in Figs. 15(a), 15(b), and 15(c), respectively, where filled circles indicate having light signals and hollow circles indicate having no light signals. It can be noted from Figs. 15(b) and 15(c) that both simulation and experimental results are $(01\bar{1}0)_{MSD} = (2)_{10}$, which are obviously correct.

6. SUMMARY AND CONCLUSIONS

In this paper, we discuss the characteristics of three stages of operations of MSD addition, and on this basis we propose a space-position-logic-encoding (SPLE) scheme that not only makes best use of the convenience of binary logic operation but is also suitable for the trinary property of 1, 0, and $\bar{1}$ in MSD digits. According to the truth tables of all the operations of MSD addition, we propose a unitary optoelectronic switch module including nine detecting elements (G_1, \dots, G_9) to implement nine AND operations of any truth table, and on this basis we build the simplest butterfly architecture of an optically fully parallel MSD adder and subtractor. This butterfly network is two dimensional; one dimension is for implementing the interconnection among operand bits, which is completed electrically within switch modules now and will be completed optically in our next work, and the other dimension is the simplest butterfly form for implementing the interconnection of two groups of operand digits in one bit, which is now completed optically. Finally, the simulation and the experimental results of MSD addition and subtraction are given. Therefore we have implemented the effective combination of a parallel carry-free algorithm (MSD) and a parallel implementing architecture (optical multilayer butterfly interconnection), which is a new approach of digital optical computing.

7. REFERENCES

1. B. L. Drake, R. P. Bocker, M. E. Lasher, R. H. Patterson, and W. J. Miceli, "Photonic computing using the modified-digit number representation," *Opt. Eng.* **25**, 38-43(1986).
2. K. Hwang and A. Louri, "Optical multiplication and division using modified-signed-digit symbolic substitution," *Opt. Eng.* **28**, 364-372 (1989).
3. Y. Li and G. Eichmann, "conditional symbolic modified signed-digit content-addressable memory logic elements," *Appl. Opt.* **26**, 2328-2333 (1987).
4. A. K. Cherri and M. A. Karim, "Modified-signed digit arithmetic using an efficient symbolic substitution," *Appl. Opt.* **27**, 3824-3827 (1988).
5. G. Eichmann, A. Kostrzewski, D. H. Kim, and Y. Li, "Optical higher-order symbolic recognition," *Appl. Opt.* **29**, 2135-2147 (1990).
6. K. H. Brenner and A. Huang, "Optical implementation of the perfect shuffle interconnection", *Appl. Opt.* **27**, 135-137 (1988).

7. J. Jahns and M. J. Murdocca, "Crossover networks and their optical implementation," *Appl. Opt.* **27**, 3155-3160 (1988).
8. F. B. McCormick and M. E. Prise, "Optical circuitry for free-space interconnections," *Appl. Opt.* **29**, 2013-2018 (1990).
9. D. G. Sun, Q. Xiang, N. X. Wang, and Z. H. Weng, "Butterfly interconnection implementation for an n-bit parallel adder/subtractor," *Opt. Eng.* **31**, 1568-1575 (1992).
10. D. Sanger and E. Wihardjo, "Parallel optical logic gates using one-dimensional spatial encoding," *Opt. Eng.* **29**, 690-695 (1990).