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A novel Si substrate mode based wafer scale optical clock distribution architecture

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With the advent of higher clock speeds and distributed multiprocessor computer architectures, a great deal of interest has arisen in developing techniques for synchronously distributing the clock signal over all of the processors in a computer. Synchronous global clock distribution is much more desirable than the asynchronous schemes used today because it greatly simplifies the overall computer architecture and further enhances performance. Unfortunately, at the clock speeds desired (>500 MHz) a synchronous global clock distribution system is very difficult to attain using electrical interconnects. Because of the high bandwidth inherent in optical signals and waveguides, various optical clock distribution schemes have been proposed to alleviate this problem. Of the techniques proposed so far, some utilize DCG gelatin volume holographic gratings at 0.632 μm[1] and light propagation in the substrate mode of a glass slab to achieve a large number of fanouts, while other techniques use surface relief gratings working in a reflection mode[2] to achieve comparable results using semiconductor fabrication techniques.

In this paper we demonstrate a novel Si wafer based optical clock distribution technique operating 1.3 μm and based on a central polygonal input coupling grating structure and surrounding rings of linear output coupling gratings shown as in figure 1. In this arrangement, both the central polygonal and linear output gratings have a period of 1 μm, allowing light to be efficiently coupled into and out of the Si wafer substrate mode in the surface normal direction. A double side polished Si wafer is used to limit the surface scattering losses as the signal travels through the bulk of the Si wafer. One of the major advantages of this technique is that, since the gratings can be written onto the Si surface using optical contact lithography and reactive ion etching, an array of grating shapes and depths can be selected to optimize the diffraction efficiency and focus the output beams onto the associated multi-chip module (MCM). This helps to reduce the optical power requirements that a future system would have and also allows for greater flexibility in system packaging design.

Figure 2 is an infrared photograph of a prototype device in operation. In order to make scattering from the gratings visible, a 350 mW, 1.3 μm Nd:YAG laser with an elliptical beam polarization is focused onto the center square grating of the device. This particular device was fabricated in a single lithography and etch step with the etch time set to produce a grating depth of 0.3 μm,

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optimizing the coupling efficiency into the substrate. For this case, 65% of the light incident on the polygonal grating is coupled into the substrate. Of the remaining 35%, 25% of the incident power was in the zeroth order reflected mode and 10% was transmitted through the device. The washed out areas visible on the edges of the wafer are due to the scattering that occurs as this input power is incident on the edges of the Si sample. In this prototype, each of the beams from the four nearest output coupling gratings can be readily observed.

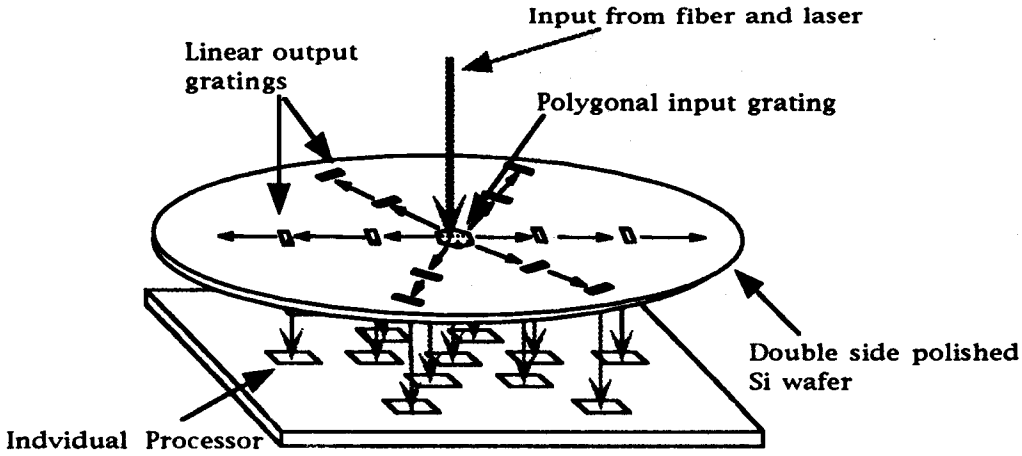

Figure 1: Schematic of Si wafer based optical clock distribution system. The clock signal is input onto the center grating via an optical fiber and laser . It is then distributed to the elements of the multi chip module via an array of surface relief gratings.

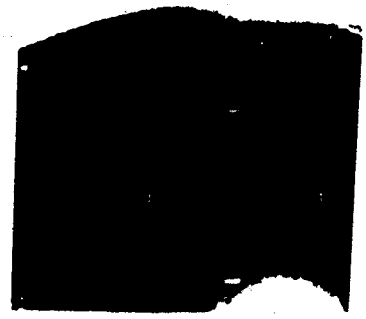

Figure 2: IR photograph of a prototype device in operation. This device is constructed with a 1 μm period and a 4 sided center grating.

The process used to fabricate the gratings in figure 3 is as follows. The pattern itself was generated using Auto CAD and additional software written specifically for this application. This pattern was then sent to a commercial mask manufacturer where it was placed on a chrome/glass photolithography mask using an electron beam direct write method. The pattern was then transferred to AZ-5209-E photoresist coated Si wafers using optical contact lithography. After exposure, the coated and patterned wafers were developed and then baked at 90 °C for 1/2 hour to

harden the photoresist so that it can be used as a mask for reactive ion etching. The wafers were then etched using RIE with Freon 114 and He as the active gasses. This fabrication process results in a rectangular grating profile whose depth can be controlled through the RIE etch time. Figure 4 gives an SEM photograph of a typical grating profile attained with this technique. In using this technique with 1 μm period gratings, careful process control must be used to insure that the photo resist is removed all the way down to the wafer in the exposed stripes of the grating. Furthermore, we also found that the moderate photoresist reflow that occurs during a standard 120°C post bake is sometimes enough to destroy gratings with the shorter 1 μm periodicity.

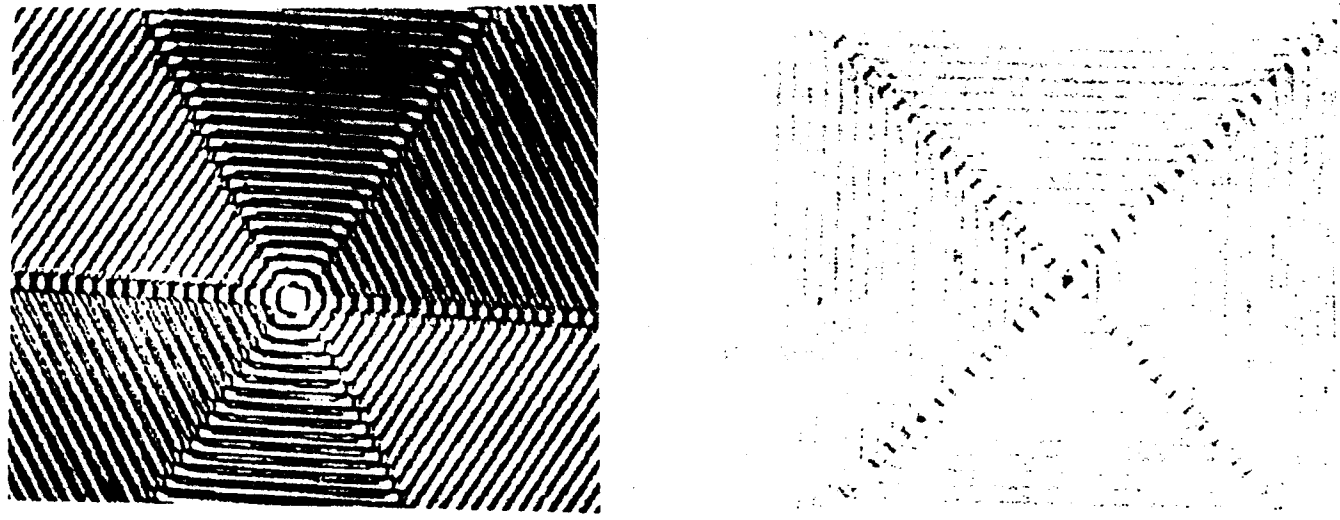

Figure 3a: Microscope photograph of the 2 μm period input coupling hexagonal grating structure in silicon used to create a 1 to 6 fanout in the substrate. 3b: 1μm period square grating structure used to create the 1 to 4 fanout in the prototype device of figure 2

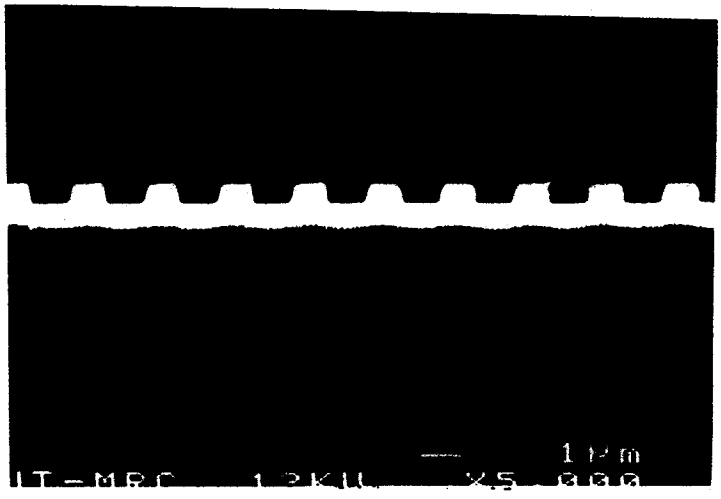

Figure 4: Scanning electron microscope picture of a 2 μm period grating after 120 second etch time. The approximate etch depth is 0.5 μm

In order to further verify the feasibility of utilizing substrate modes in double side polished Si, propagation loss measurements were made using a cutback method. Samples of double side polished Si of increasing length were prepared by cleaving both ends of each sample. Laser light at 1.3 μm was then end coupled into and out of the samples and focused onto a photodetector. The major source of error encountered in using this technique, were small imperfections in the cleaves present at the sample ends. These imperfections can cause perturbations in the loss measurements that are often greater than the loss itself. The result of this measurement is given in figure 2. The slope of this line corresponds to a substrate mode loss of 0.39 dB/cm. The loss due to bulk absorption at 1.3 μm in Si is 0.03 dB/cm, indicating that the primary source of loss in Si substrate modes is irregularities in the material, either at the surface due to dirt or in the bulk due to small defects in material's crystalline structure.

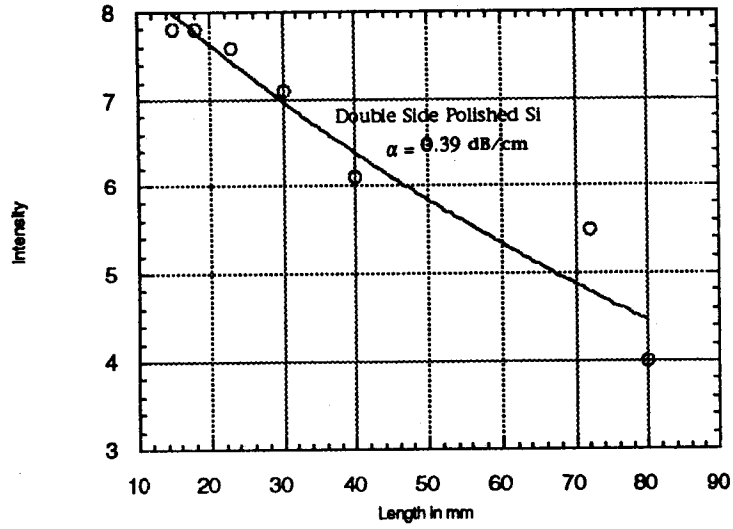

Figure 5: Output coupled intensity of Si substrate modes for samples of different length.

The diffraction efficiency of a set of 2 μm period gratings was measured as a function of etch time for three different wavelengths: 0.632, 1.06, and 1.32 μm in reflection mode. This was done in order to investigate the influence of the actual depth of the fabricated gratings on the grating efficiency and determine the optimal etch depth. Using 2 μm period gratings instead of the 1 μm period of the device allowed us to measure diffraction efficiency using the 1st diffracted order. When the diffraction efficiency is assumed to have the approximate form of a rectangular reflection grating [4],[5] the efficiency has the dependence:

$$\eta \propto \sin^2\left(\frac{2\pi d}{\lambda}\right)$$

As can be seen from the data in figure 6 the peak diffraction efficiency in figure 6 occurs at an etch depth of 0.3 μm and for an etch time of 90 seconds. Furthermore, our measurements of diffraction efficiency for all three wavelengths explored allow us to make an estimate of the grating

depth at various etch times. In particular, for the 120 second etch time, the etch depth obtained from the diffraction data agrees with the depth from the SEM grating profile shown in figure 4. Table 1 below gives the calculated etch depths for the minima and maxima of grating efficiency at the various etch times. From this table one can develop a good picture of grating depth vs etch time to use in grating efficiency optimization.

wvlth µm	min eff time	calc depth µm	max eff time	calc depth µm
1.32	90	0.32	130	0.65
1.06	80	0.25	120	0.53
0.063	40	0.15	90	0.32

Table 1: Calculated grating depths at the minimum and maximum efficiency etch times for all three of the wavelengths used in the experiment.

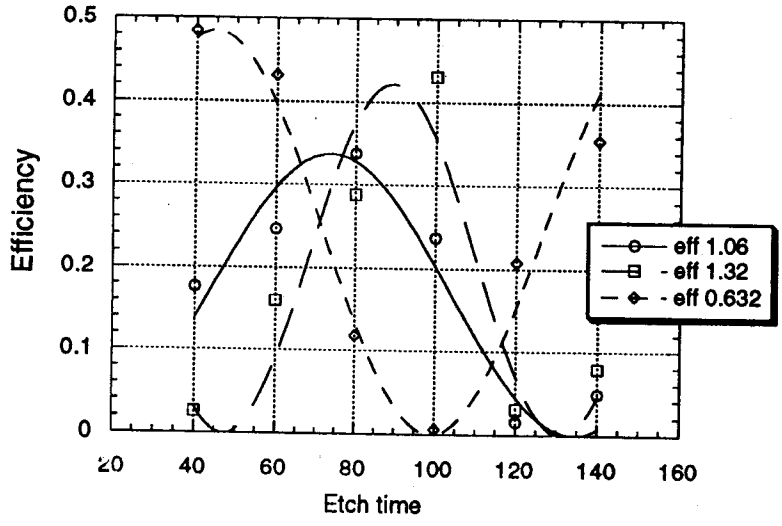

Figure 6:Grating efficiency vs etch time for 0.632 1.06 and 1.32 µm.

We are also working to develop an optical clock distribution system based on Si-Ge waveguides. The form of this system is analogous to that of the Si substrate mode system except now an H-tree[6] configuration of Si-Ge waveguides will be used instead of the polygonal grating structure on the Si substrate. The Si-Ge layer used will be 5 µm thick with a Ge concentration of 4%. The waveguide width that will be used is 100 µm, which is intended to match the near field pattern of a multi-mode optical fiber. Coupling into the Si-Ge waveguide will be realized using a surface relief diffraction grating. These large waveguide widths will also allow the construction of 90 ° bends and splitters similar to those already demonstrated in [7]. Figure 7 shows a microscope picture of some of the first waveguides we have constructed in this configuration. Further results will be presented in a future publication.

Figure 7: 90° bend and 3 dB splitter configuration used in 100 μm width Si-Ge waveguides

In conclusion, we have demonstrated a novel architecture for a 1.3 μm optical clock distribution system. This architecture is based on 1 μm period rectangular profile gratings patterned using optical contact lithography and RIE. This fabrication technique should allow the grating depth and form to be manipulated, allowing control of the output beam focusing and coupling efficiency. Using this method, a prototype device with an input coupling efficiency of 65% was demonstrated. Furthermore, the loss of the Si substrate modes was measured at 0.39 dB/cm. As a result, this Si wafer based optical clock distribution architecture represents a viable design alternative that should be explored further.

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