Planar Formation of 3-D highly Parallel Optical Fan-out Interconnects for Wafer Scale Optical Clock Signal Distribution

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Abstract

In this paper, we present a miniaturized compact three-dimensional optical fan-out interconnect suitable for wafer scale VLSI multichip module optical clock signal distribution. The demonstrated device employs a thin light-guiding substrate in conjunction with a two-dimensional optical hologram array. The parallel feature among fan-out beams and the planar compact structure convert the un-solvable three spatial and three angular multiple alignment problem into a single-step 2-D planar one, which greatly enhances the packaging reliability. New design scheme for minimizing throughput power non-uniformity is presented for the first time. A 25 GHz 1-to-42 highly parallel fan-out interconnect was demonstrated with a signal to noise ratio of 10 dB.

1. Introduction

The speed and complexity of integrated circuits are increasing rapidly as integrated circuit technology advances from very large scale integrated (VLSI) circuits to ultra large scale integrated (ULSI) circuits. As the number of components per chip, the modulation speed and the degree of integration continues to increase, electrical interconnections are facing their fundamental bottle-necks, such as speed, packaging, fan-out, and power dissipation. Multichip module (MCM) technology is employed to provide higher clock speeds and circuits densities[1,2]. But the state-of-the-art electrical interconnection and packaging technologies still fail to provide the required clock speeds and communication distances in intra-MCM and inter-MCM hierarchies. For example, with a clock speed of 1-GHz, electrical interconnects can only provide us with ~1 cm communication distance[3-5]. High speed massive fan-out optical interconnects outperform electrical interconnects in these interconnection scenarios[3-9]. For clock signal distribution in MCM, a successful interconnect should employ little real estate of the semiconductor wafer surface that has already been intensively occupied by electronic devices[1,2]. An array of novel optical interconnects using substrate guided wave and/or free-space in conjunction with holographic elements, have been proposed and then reported by earlier researchers[10-13], which may satisfy the above requirements for wafer scale clock signal distribution in MCM.

In this paper, we present the demonstration of an unique 3-D free-space compact optical parallel fan-out interconnect for massive clock signal distribution in MCM. Unlike the previously proposed work[9-14], an integrated wafer scale optical interconnect with 1-to-42 (6x7) parallel fan-outs is realized, using a thin light-guiding substrate in conjunction with a 2-D optical hologram array fabricated on its surface. More importantly, the parallel feature among fan-out beams and the planar compact device structure convert the un-solvable three spatial and three angular multiple alignment problem into a single step 2-D

planar one. The device demonstrated herein minimizes the employment of real estate of semiconductor surface. Better device architecture is presented to increase fan-out and to improve the intensity uniformity among optical fan-out beams compared with our previous work[15]. A 25 GHz integrated 1-to-42 highly parallel optical fan-out interconnect is demonstrated experimentally in this paper. Such a device is pivotal for miniature, compact, massive fan-out interconnect systems using planar integration technology. In fact, the demonstrated device can be fabricated by using techniques originally developed for manufacturing VLSI semiconductor circuits and/or techniques for manufacturing optical holograms.

2. Theory

The schematic of the optical interconnect presented is shown in Fig. 1. It consists of a thin glass substrate in conjunction with a 2-D optical grating array fabricated on its surface. These optical gratings can be fabricated directly on the semiconductor substrate surface using standard VLSI fabrication technologies. For demonstration purpose, the 2-D grating array is an optical hologram array made out of a thin dichromated gelatin (DCG) film coated on a thin glass surface. The thin glass is employed as a light-guiding plate. The hologram array consists of holograms of h_o, h_n and multiplexed holograms of h_{mn}. The h_o is the input coupler designed to couple the surface normal input laser beam into a substrate guided beam with bouncing angle θ_m. The multiplexed h_{mn}, having two gratings h_{mn1} and h_{mn2}. h_{mn1} is designed to fan-out the input substrate guiding beam into a linear array of surface normal fan-out beams with coupling efficiency η_{mn1}. h_{mn2} with coupling efficiency η_{mn2} is designed to deflect the substrate guiding beam into a linear array of substrate guided beams with bouncing angle θ_n. Both θ_m
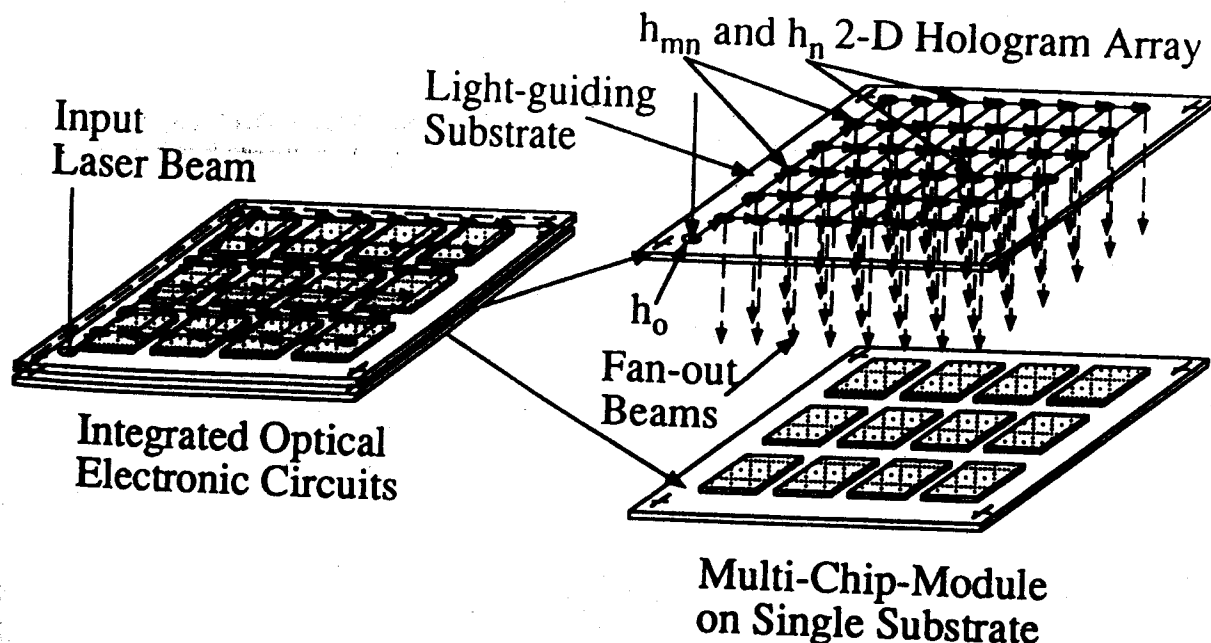

Fig. 1. Schematic of the proposed optical interconnect for MCM clock distribution.

and θ_n (not shown in Fig. 1) are larger than the critical angle of total internal reflection (TIR) of the substrate. h_n is designed to couple the array of substrate guiding beams into a 2-D array of surface normal fan-out beams with coupling efficiency η_n. As the results, highly parallel massive fan-out beams are created inside the light-guiding plate together with surface normal massive fan-out beams, which are also parallel to the input laser beam. It can be seen that any permutation can be arranged without blocking guided-wave propagation inside the light-guiding substrate, in three global routing steps; permuting through input hologram (h_o), then through deflecting hologram (h_{mn2}) and finally through output hologram (h_n).

Note that h_{mn1} may not be needed in order to simplify and improve the device design and fabrication. Through gradually increasing the coupling efficiency, i.e., increasing the hologram index modulation along the fan-out beam sequences, uniform intensity among the fan-out beams can be realized. The method to construct the holograms was detailed in our recent publication of Ref.[8]. The advantage of the presented device is the index (~1.5) match between the thin glass substrate and DCG film. Thereby the substrate guided beam through TIRs interacts with the holograms on the glass surface.

Minimization of the throughput non-uniformity of fan-out beams is an important design concern, which is determined by the arrangement of the 2-D holograms and their coupling efficiencies, of course, the number of fan-out beams as well. The output power of a fan-out beam in the demonstrated device can be precisely calculated. For example, for the 1-to-42 fan-out interconnect reported herein, the output power can be written as

$$I_{m1} = I_o\eta_o\eta_{mn1}(1-\eta_{mn1}-\eta_{mn2})^{m-1} \qquad\qquad m = 1, 2, 3, ... \qquad (1)$$

$$I_{mn} = I_o\eta_o\eta_n(1-\eta_{mn1}-\eta_{mn2})^{m}(1-\eta_n)^{n-1} \qquad\qquad n = 2, 3, 4, ... \qquad (2)$$

where I_o is the power of input beam, m and n stand for, respectively, the sequence of columns and rows of the 2-D array of the parallel fan-out beams. As indicated by Eq. (2), a tradeoff exists between the fan-out power and the grating fan-out efficiencies. Optimum values of η_n in designing a 2-D hologram array with maximum throughput power for the weakest fan-out beam, corresponding to minimum power non-uniformity among fan-out beams, can be derived from Eq. (2). For example, for a 1-to-42 device with $\eta_{mn1} = \eta_{mn2} = 10\%$, the optimum coupling efficiency is around $\eta_n = 15\%$. Note that the reflection and scattering loss is not included in Eq. 2. The diffraction efficiency of a hologram can be accurately controlled experimentally[8,9,15]. In our experiments, coupling efficiency is consistently adjustable up to 70%. The presence of each fan-out hologram can be designed and then fabricated independent. As the result, the presence of each fan-out beam can be arranged in design. The propagation loss of the glass was determined to be less than 0.1 dB/cm experimentally. Thereby, large scale fan-out device can be provided.

3. Experimental Results

Fig. 2 is a photograph of surface normal 1-to-42 highly parallel optical interconnect using a glass substrate, integrated with a 2-D multiplexed hologram array. The holograms were fabricated at working wavelength of 632.8 nm, where $\eta_o = 70\%$, $\eta_{mn1} = \eta_{mn1} = 10\%$ and $\eta_n = 19\%$ were experimentally

confirmed. In this photograph, a surface normal free-space HeNe laser beam (9 mW) is coupled into the glass substrate through the surface normal input hologram η_0. The parallel fan-out beams are generated by the 2-D hologram array either propagating along the substrate or normally coupling out off the substrate. The far field pattern of the 42 surface normal fan-out beams is also displayed in Fig. 2.
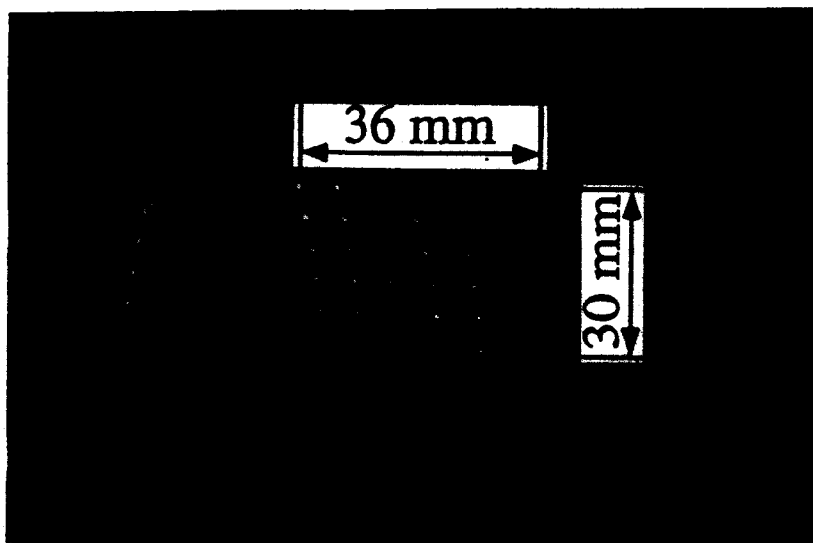

Fig. 2. Photograph of surface normal 1-to-42 highly parallel optical fan-out interconnect. The far field pattern of fan-out beams is also shown.

Note that the mode dots preserve the azimuth symmetry of TEM_{00} beam of the input laser. As a result, coupling to a 2-D photodetector array will be much easier when compared with the conventional single-mode guided wave devices. Fig. 3 is the measured optical throughput of the 42 surface normal fan-out beams.
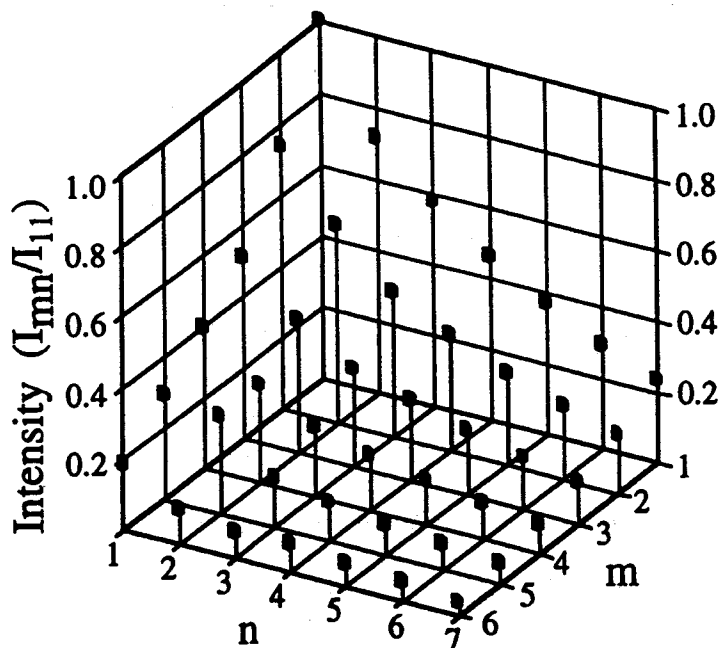

Fig. 3. Measured optical throughput of the 42 fan-out beams.

In designing massively parallel optical fan-out interconnect shown in Fig. 1, the fan-out packing density is another important parameter of system performance. The fan-out packing density is determined by the substrate thickness, substrate guided beam bouncing angles θ_n and θ_m as well as the angle α between the two projection of holographic grating vectors of h_o and h_{mn2} on the surface of a glass substrate. We select $\alpha = 90^o$ and set $\theta_n = \theta_m = \theta_d = 45^o$ for symmetric purpose. Therefore, the separation between any two nearest fan-out beams is given by

$$s = (2t)\tan(\theta_d) , \qquad\qquad (3)$$

where t is the thickness of the glass substrate. By selecting the glass thickness and/or coupling angles, the desired packing density of fan-out beams can be obtained. The location of the fan-out beams can be easily determined as $(x_m, y_n) = (ms, ns)$, where m, n = 1, 2, 3....

The angular alignment tolerance of the input beam is another important concern. Fig. 4 shows the experimental results of the diffraction efficiency of a fan-out beam (3, 3) versus input angle misalignments of the fan-out device shown in Fig. 2. The angular full-width at half-maximum of the maximum diffraction efficiency is $\pm 1^o$, which indicates that it has a large angular tolerance of $\pm 0.5^o$ before a significant drop of diffraction efficiency.
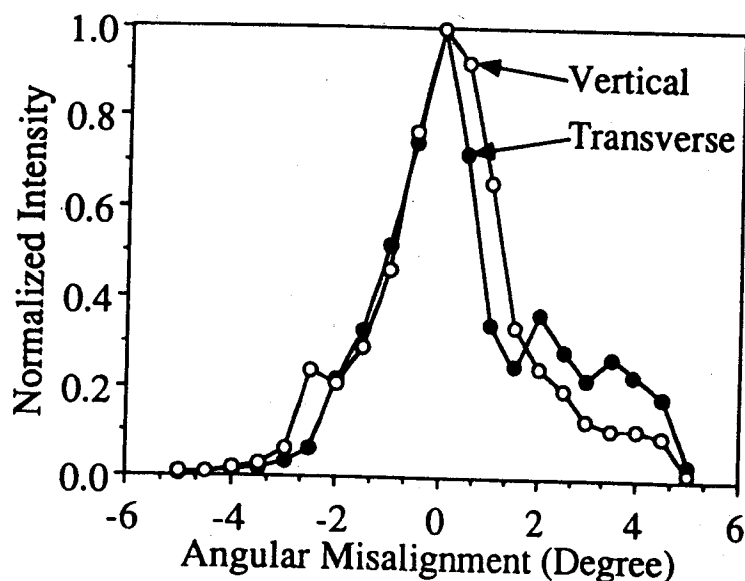

Fig. 4.   Experimental results of fan-out efficiency versus angular misalignment of input beam. The two rotation ax are perpendicular to each other and perpendicular to the input beam as well.

The input beam angular misalignment will also cause a spatial shift of fan-out beam due to the shift of diffraction angle θ_d within the substrate. Based on the phase-matching condition, we have

$$n_s \sin(\theta_d) = \lambda/\Lambda_x - \sin(\theta_i) \qquad\qquad (4)$$

where Λ_x is the surface grating period, n_s is the substrate index, θ_d is the diffraction angle and θ_i is the incident angle of input laser beam. Differentiating Eq. (4) while holding λ fixed, we obtain

$$d\theta_d = -[\cos(\theta_i)/(n_s\cos(\theta_d)]d\theta_i. \qquad (5)$$

The resulting maximum amount of spatial shift can be determined based on Eq. (3) and (5), which is

$$\Delta L = 2t[\tan(\theta_d) - \tan(\theta_d \pm d\theta_d)]. \qquad (6)$$

For the device demonstrated herein with t = 3.0 mm, θ_i = 0° and θ_d = 45°, 0.5° and 0.05° input angular misalignments correspond to ~100 μm and ~1 μm spatial shifts, respectively. Eq. (6) indicates that the un-solvable problem of the three spatial and three angular multiple alignments is converted into a single step 2-D planar one. Standard state-of-the-art 2-D planar alignment techniques, with the resolution of ~0.1 μm developed for fabricating VLSI circuits, can be employed to integrate the demonstrated device to a Si VLSI multichip module.

An optical coherent beating signal was employed as the optical clock signal[16]. By co-propagating two single longitudinal laser beams (HeNe laser of λ_1 = 632.80 nm and dye laser of λ_2 = ~632.83 nm) through the 1-to-42 fan-out interconnects fabricated, a beat signal equivalent to an optical wave modulated at a microwave frequency of 25-GHz, was detected at the weakest fan-out (6, 7) and the result is shown in Fig. 5. A signal-to-noise ratio of 10 dB is observed.
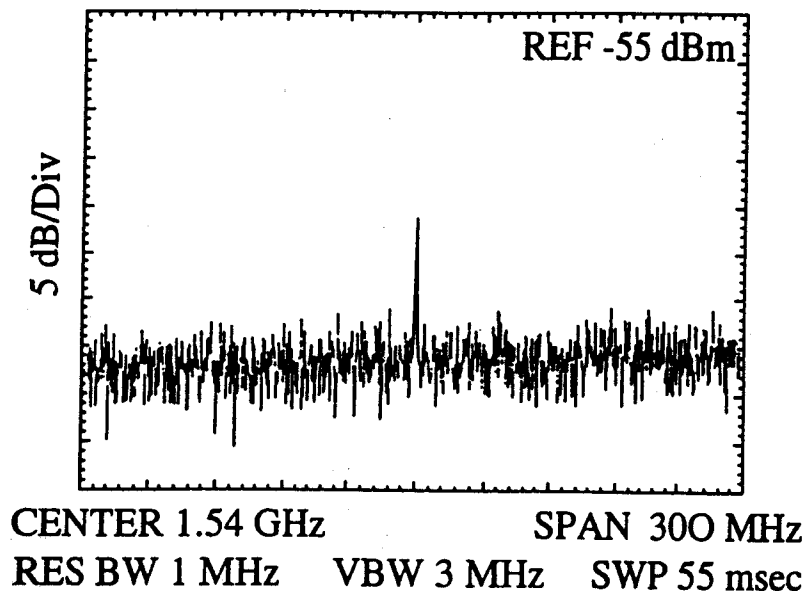

Fig. 5.   25-GHz optical beating signal through the optical fan-out interconnect shown in Fig. 3, obtained from the weakest fan-out beam (6, 7).

4. Concluding Remarks

In summary, we represent the first effort to construct a 3-D integrated free-space compact optical fant interconnect for wafer scale fast clock signal distribution. The power uniformity among fan-out ams, the number of fan-out were significantly improved through better design of 2-D holograms, mpared with our previous work[15]. It was shown that the difficulties associated with the mplicated 3-D multiple alignments are significantly reduced through the parallelism among the fan-out ams and the unique planar device feature. 25-GHz clock signal was demonstrated experimentally for ε first time with 42 parallel fan-outs.

5. Acknowledgment

6. References

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