Thick Phase Hologram for Optical Clock Distribution Application on Wafer Scale Integrated Circuits

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ABSTRACT

We propose the first monolithic optical clock distribution network on wafer scale integrated circuits (WSIC). This new architecture can save real estate on VLSI chips and eliminate the packaging, alignment and interface problems of previously proposed architectures. A 1-to-3 optical fan out for clock signal distribution application is demonstrated by utilizing a DCG multiplexed volume hologram on a thin quartz plate.

2. INTRODUCTION

Electrical switching and interconnects have been identified as deadlocks to the throughput of computing and signal processing systems. Research on new architectures for increasing the parallelism and, therefore, the throughput of a computing system is in great demand. One area where optical interconnects can increase system performance is where large fanouts are needed over speeds and distances required for high performance processors. Numerous examples of high fanout interconnects in signal processing and computing architectures occur at the intra and interboard level, including clock distribution, optical bus and monitor. The use of optical interconnects suitable for wafer scale integration (WSI) can remove most of these restrictions on array architecture.

Integration at the wafer level is the final degree to which monolithic device fabrication can be realized. High circuit packaging density and the removal of constraints on the segmentations of a system into chip size blocks make the performance of WSI very attractive.

Optical clock distribution has been identified as the most promising application of intra wafer optical interconnect (IWOI)[1,2]. The architectures proposed by Goodman[3] and Bergman[4] utilize a multiplexed hologram which is located on top of an IC chip surface. A laser diode is located on top of the multiplexed hologram. This kind of architecture is not practical because it is bulky and the alignment of these discrete components is extremely difficult. Furthermore, the multi-layer structure requires that packaging technology also be upgraded. The architecture proposed by Hartman[5] involves fiber and optical waveguides. The interface problem and the limitation of real estate makes this architecture impractical.

3. EXPERIMENTS

We report a monolithic optical clock distribution network on a wafer scale integrated circuit. The alignment problems are eliminated by integrating light

sources, multiplexed volume holograms, and detectors on the same substrate. This substrate can be a semi-insulating GaAs wafer. The new architecture is shown in Fig.1. Contrary to the holoplanar interconnects, which route the optical signal in coplanar geometry, the multiplexed hologram we introduced here can couple optical clock signal in the vertical direction. This type of hologram is sometimes referred as a total internal reflection (TIR) hologram. In this architecture, a surface emitting laser diode is grown on the top surface of the wafer and the multiplexed hologram is attached to the bottom surface of the same wafer. The energy of the photons emitted by the surface emitting laser diode is designed to be less than the band gap E_g of the host material. Therefore, low loss propagation in the substrate region becomes possible. The multiplexed transmission hologram which routes the clock signal is recorded using the setup shown in Fig.2. Multiple gratings are formed by rotating the holographic plate and changing the recording beam incident angles after each exposure. To form a slanted grating coupler which converts vertical incident wave to a total internal reflection mode with bouncing angle Φ (between surface normal and diffracted wave propagation direction), the two incident angles of the recording beams (Fig.3) are

$$\theta_1 = \sin^{-1}(n/n_r(\sin(\delta))) \tag{1}$$

$$\theta_2 = \sin^{-1}(n/n_r(\sin(\Phi-\delta))) \tag{2}$$

where n is the index of refraction of the DCG volume hologram and n_r is the refractive index of the medium on top of the DCG hologram (n_r=1 for air) and

$$\delta = \Phi/2 - \sin^{-1}(\lambda_b/\lambda_r(\sin(\Phi/2))) \tag{3}$$

In Eq.(3), λ_b and λ_r represent the wavelengths of recording and reconstructing waves, respectively.

To increase angle Φ, i.e., increase the distance of the optical clock distribution signal, we can either decrease the ratio of λ_b/λ_r by changing the recording and reconstructing wavelengths or increase n_r by putting a high index prism right in the front of holographic plate.

Since the thickness of a typical semiconductor wafer is ~300 μm and the integrated passive and active devices are only a few μm deep (up to ~10 μm) on the top surface, the remaining volume is not effectively used. In this new architecture these unused areas are employed as the optical path to route the optical clock signal. In GaAs MMIC, the Ohmic contact is made on the same surface as the other integrated devices (FETs, diodes, etc). Accordingly, no electrooptic cross coupling exists in this new architecture.

A 1-to-3 optical fan-out for clock distribution application based on an integrated multiplexed hologram is shown in Fig.4(a). In this photograph, a thin quartz plate is used to demonstrate the feasibility of this novel architecture. The multiplexed volume hologram is recorded with the set up shown in Fig.2. The schematic representation of the reconstruction geometry is shown in Fig.4(b). A He-Ne laser operating at 632.8nm is used for this demonstration. The photograph shown in Fig.4(a) was taken by a CCD camera. A 1-to-3 fanout to route the optical clock signal is clearly observed.

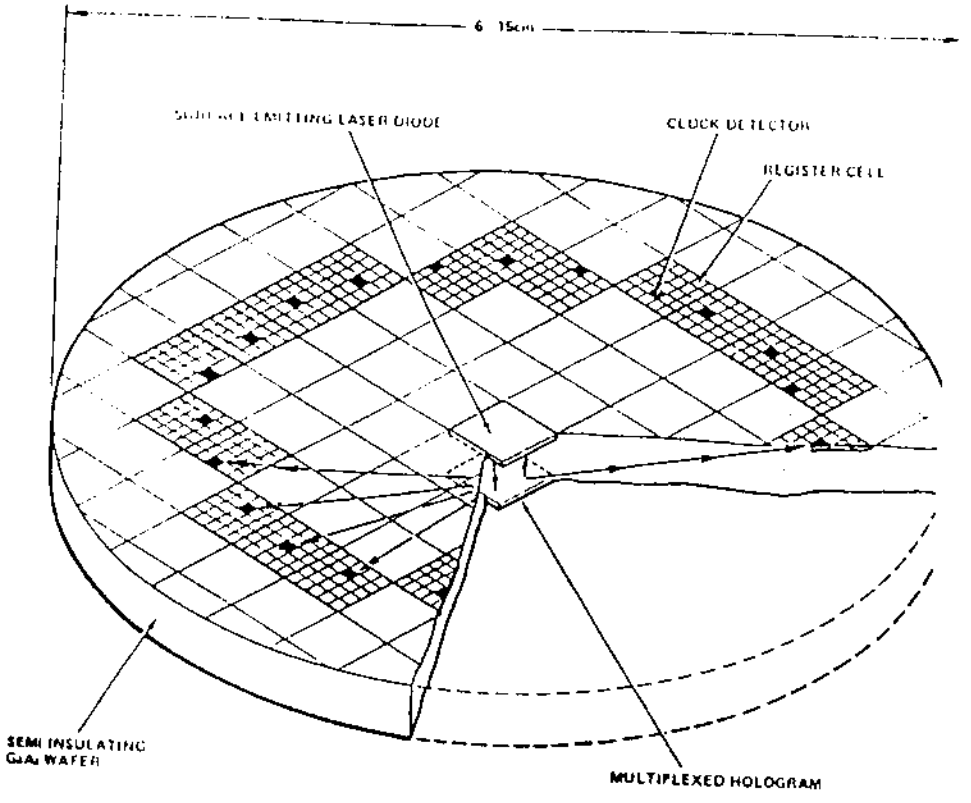


Fig.1 Optical Clock Distribution on Semi-Insulating GaAs Wafer Scale Integrated Circuits (WSIC)

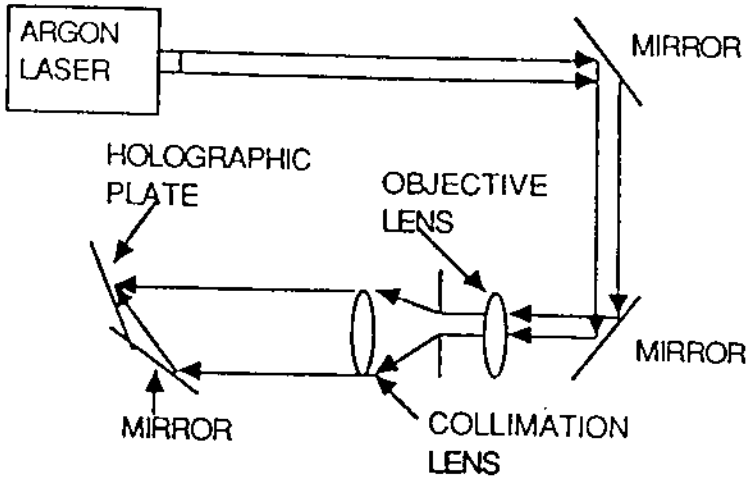


Fig.2 Recording Setup of the Multiplexed Volume Hologram to Route an Optical Clock Signal

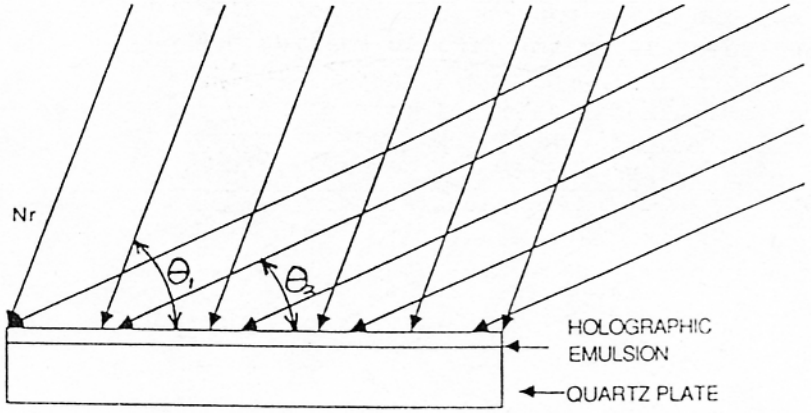
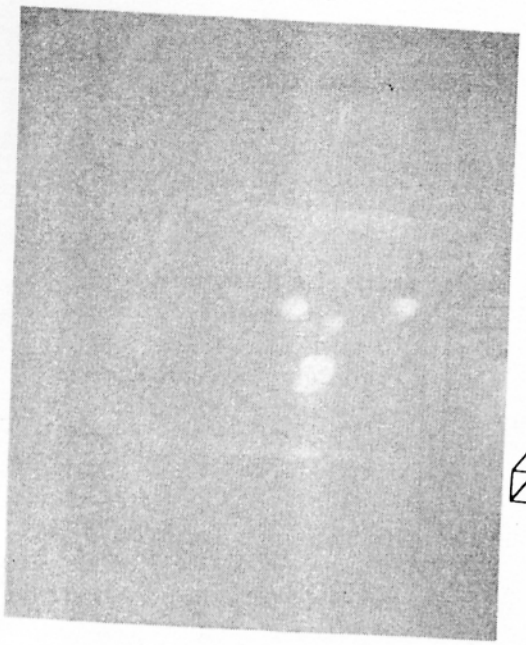


Fig3. Schematic Representation of the Recording of a Transmission Hologram



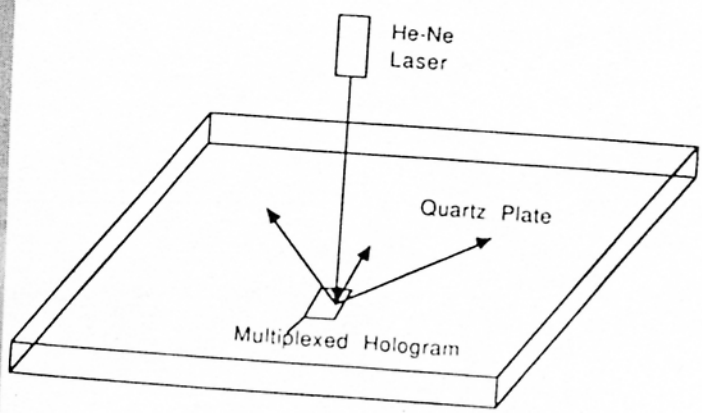


Fig.4(a) 1 to 3 Optical Fan out for Clock Distribution Application through Multiplexed Volume Hologram on a Thin Quartz Plate (b).Reconstruction Geometry of Fig.4(a)

In this experiment, the angular width $\Delta\Theta_{Bragg}$ of the Bragg response between half power point is[6]

$$\Delta\Theta_{Bragg} = \lambda_r/T \qquad (4)$$

for transmission gratings. In Eq.(4), T is the thickness of the hologram which is ~85 μm. We have $\Delta\Theta_{Bragg}$ ~10^{-2} Rad. Therefore, a 1 to 100/rad fanout is theoretically feasible with this new architecture.

4. CONCLUSION

We describe a new optical clock distribution network on wafer scale integration (WSI) which combines laser diodes and multiplexed holograms onto the same wafer. Such an architecture can save the real estate of VLSI chips and eliminate the packaging, alignment and interface problems of previously proposed architectures. A 1 to 3 optical clock distribution on a thin quartz plate has been demonstrated for the first time. Further theoretical calculation shows that a 1 to 100/rad fanout is plausible with this new architecture.

5. ACKNOWLEDGEMENTS

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6. REFERENCES

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