System demonstrator for board-to-board level substrate-guided wave optoelectronic interconnections

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ABSTRACT

We design and implement a system demonstrator based on vertical-cavity surface-emitting lasers, polymeric hologram grating couplers, and metal-semiconductor-metal photodetectors. As a preliminary experiment, we show the feasibility of board-to-board level substrate-guided wave optoelectronic interconnections in the real electrical system. First, we introduce a new architecture – centralized optical backplane – for board-to-board level interconnections. Second, the optoelectronic data channel is constructed compatible with standard PECL and capable of operating at 1.25 Gbps. Finally, it is employed to replace the conventional electrical data channel in a microprocessor system. We describe the performance of the entire system and discuss the future application of our centralized optical backplane in other electrical systems.

Keywords: substrate-guided wave, optoelectronic interconnections, centralized optical backplane

1. INTRODUCTION

Optical interconnections are now being intensively studied at various levels of the interconnect hierarchy. The hierarchy of interconnect problems is a very important concept. An interconnection solution at one level may not be suitable, or even workable at another level. Finding a proper role for optics at each level of the hierarchy is a challenging research problem of the day. In long-distance telecommunications, fiber optics has been the dominant technology. In short-distance data communications, optical technologies have not moved into the mainstream yet. However, as the speed and complexity of data communication systems continue to increase, electrical interconnections are facing their fundamental bottlenecks. Intrinsically high bandwidth and potentially low latency make optical interconnections promising technologies for both evolutionary and revolutionary changes in data communications.

In this paper, we describe the concept of centralized optical backplane and its application to microprocessor-to-memory interfacing. To justify this solution, we design and implement a system demonstrator based on vertical-cavity surface-emitting lasers, polymeric hologram grating couplers, and metal-semiconductor-metal photodetectors. The performance of the entire system is described in this paper.

2. CENTRALIZED OPTICAL BACKPLANE

Figure 2.1 shows the schematic diagram of centralized optical backplane. The active optoelectronic modules, including transmitters and receivers, are placed on the backside of the electrical backplane board. The board inserted into the center slot of the electrical backplane board plays an important role in this architecture and is named Center in this paper. The design of the optical signal path is based on substrate-guided wave optics [1]. One double grating hologram is attached on the top surface of the substrate and positioned just below the active optoelectronic module of the Center. Other boards have similar configurations, but (1) the positions of transmitters and receivers are switched, and (2) single grating holograms are used. There are two optical signal paths, one is for a board to deliver signals to the Center, as shown in figure 2.2 (a), and the other one for the Center to broadcast signals to all boards, as shown in figure 2.2 (b).

For a complete data transaction from one board to (1) another board (point-to-point), (2) a number of other boards (multicast), or (3) all the other boards (broadcast), two processes are involved. First, the optical signal from the source board

is coupled into the substrate through the single grating hologram. It propagates within the substrate as substrate-guided wave, and then coupled out of the substrate through the double grating hologram of the Center. Second, the active optoelectronic module of the Center regenerates the same signal and sends it back into the substrate. The optical signal is split by the double grating hologram into two identical signals propagating along two opposite directions as substrate-guided waves. During the propagation, a certain portion of the optical signal is coupled out of the substrate through the single grating hologram and processed by the corresponding active optoelectronic module. Thus bi-directional broadcasting is implemented.

For a broadcasting architecture, it is desirable to get even fan-out, because the non-uniformity of fan-out powers makes it more difficult to integrate optical detector arrays and other optical signal processing elements. In the centralized optical backplane, even fan-out is achieved by proper design of diffraction efficiencies of single grating holograms as discussed by our research group (to be published in this proceeding).

3. DESIGN AND FABRICATION OF HOLOGRAMS

We choose photopolymer film (HRF-600X001-20) from DuPont Holographic Materials to fabricate grating couplers. The HRF-600X001-20 is suitable for this application because of its dry-processing capability, long shelf life, good photospeed, and high index modulation. The grating formation process in dry photopolymer materials can be well described by the diffusion model [2]. The photopolymer film consists initially of monomers, polymeric binders, and photoinitiators. When exposed to light, the monomers are polymerized and the percentage of polymerized monomers increase with the exposure. Therefore, when the photopolymer film is exposed to an interference pattern, the distribution of monomers being polymerized forms the same pattern as the exposing interference pattern. This non-uniform distribution sets up monomer concentration gradients, and hence results in diffusion of monomers from dark regions to the neighborhood bright regions. Thus, a polymer density spatial distribution is formed which results in a refractive index modulation (grating) of a same pattern. A final uniform exposure is used to polymerize the remaining monomers and stabilize the grating. According to the coupled wave theory [3], the diffraction characteristics of a volume hologram at first-order Bragg angle are essentially determined by the first-order grating. In order to get a grating coupler with certain diffraction efficiency we need to control the exposure dosage thus the amplitude of the first-order grating. This process depends on the dynamic characteristics of photopolymer films [4]. We use real time monitoring technique to achieve the goal of diffraction efficiency control.

Figure 3.1 (a) shows the setup for single grating hologram recording. The 532 nm line of 0.25 W from a Verdi laser is used for all the exposures, and diffracted light from a 850 nm probe laser is monitored during and after the exposure. To examine the dynamic characteristics of single grating holograms, a series of single grating holograms is recorded with the exposing illumination stops before saturation is reached. Figure 3.2 shows the diffraction efficiency as a function of time during and after the exposure. The diffraction efficiency continues to increase after the termination of the exposure. The amount and speed of the increment depend on the value of the diffraction efficiency that the exposure stops at. Therefore, figure 3.2 can be used as a guide to get a single grating hologram with certain designed diffraction efficiency.

Figure 3.1 (b) shows the setup for double grating hologram recording, in which one more detector is used in order to monitor two diffracted probe beams during and after the exposure. Our goal is to get equal-strength double grating holograms, i.e., 50 / 50 beam splitter. First, the exposure is stopped when diffraction efficiency achieves some value. Second, the substrate is rotated 180^{o}. Third, we wait for some time. To ensure the repeatability of the experiments, the total time for the second and third step is 30 seconds. Fourth, the photopolymer film is exposed to the recording beams again for the second grating formation. To examine the dynamic characteristics of double grating holograms, a series of double grating holograms is recorded with the second exposing illumination, which begins with different diffraction efficiencies in the first grating. Figures 3.3 (a), (b), (c), and (d) show diffraction efficiencies of two gratings as functions of time during the second exposure. Due to the non-linearity of the fringe formation process, the formation of the second grating affects the diffraction efficiency of the first grating. Under some conditions, as shown in figures 3.3 (a), (b), and (c), it is possible to get equal-strength double grating holograms, and the diffraction efficiency of the equal-strength double grating hologram depends on the first grating's diffraction efficiency that the second exposure starts with. Under some other conditions, as shown in figure 3.3 (d), it is impossible to get equal-strength double grating holograms. Therefore, figures 3.3 (a), (b), (c), and (d) can be used as a guide to get a 50 / 50 beam splitter with maxim achievable diffraction efficiency.

Figure 3.4 shows the even fan-out from the centralized optical backplane with (a) three boards, and (b) five boards. The fan-out variation can be controlled within 2.5 %. Figure 3.5 shows the even fan-out from a multi-bus-line centralized optical backplane with five boards. The fan-out variation can also be controlled within 2.5 %.

4. DESIGN OF TX AND RX

For the transmitter design, we use VCSEL with lasing wavelength of 850 nm (VCT-B85B20) from Lasermate Corporation and laser diode driver (MAX3261) from Maxim Integrated Products. Interfacing laser diode driver circuits with commercially available VCSELs at high data rates can be a complicated and challenging task. The three major pieces of the VCSEL interface puzzle include (1) the electrical characteristics of the VCSEL, (2) the output circuit of the laser diode driver, and (3) the interface circuit between them [5]. The VCT-B85B20 is in TO-46 package. The threshold current varies from 3mA to 5mA. For fast switching operation, it is a common practice to bias the VCSEL above the threshold to avoid turn-on and turn-off delay. The typical operating current of VCT-B85B20 is 12mA. The series resistance is approximately 30 Ω. The MAX3261 is a complete, single +5 V powered, 1.25Gbps laser diode driver. It accepts differential PECL inputs and provides complementary output currents. A temperature-stabilized reference voltage is provided to simplify laser current programming. This allows modulation current to be programmed up to 30 mA and bias current to be programmed up to 60 mA with two external resistors. The interface circuits are carefully designed based on [5] and [6].

For the receiver design, we use Photodetector / Transimpedence Amplifier (VSC7810) from Vitesse Semiconductor Corporation and Post-amplifier (MAX3268) from Maxim Integrated Products. The VSC7810 is a highly integrated solution for converting a input optical signal (850 nm) into a differential output voltage. It provides high data rate (1.25Gbps) and low input noise equivalent power (1.4 μW) with a large optically active area (100 μm diameter) for easy alignment. The differential responsivity is 1.2 mV/ μW. The MAX3268 is designed for Gigabit Ethernet and Fiber Channel optical receiver systems. It accepts a wide range of input voltages (10 mV – 1200 mV) and provides constant-level output voltages (PECL) with data rate up to 1.25 Gbps.

Figure 4.1 (a) and (b) shows the printed circuit board we design and assemble as the active optoelectronic module for the centralized optical backplane. It includes two transmitters and two receivers, thus implements one bi-directional data path between two boards. The separation between one VCSEL and the corresponding Photodetector / Transimpedence Amplifier is 2.6 cm, and the distance between two signal paths is 0.5 cm. The clean and open eye, as shown in figure 4.2, justifies the module's capability of operating at date rate up to 1.25 Gbps.

5. MICROPROCESSOR SYSTEM

Figure 5.1 shows the block diagram of the microprocessor system. The control lines, which are not shown in the figure, and the address lines are conventional electrical interconnections. The data lines are replaced by our centralized optical backplane. Shift registers are used to interface 8-bit electrical data lines with 1-bit optical data line. Logic translators are used to interface TTL with PECL. Figure 5.2 shows the photo of the system.

For simple demonstration, data '0x22' (00100010) is written from the microprocessor's EEPROM to the memory, and then read back from the memory to the microprocessor's EEPROM. We measure data waveforms at test point 1, 2, and 3. Figure 5.3 shows the data waveform at the test point 1, which is the output signal from the 8:1 shift register, and the system clock. Figure 5.4 shows the data waveform at the test point 2, which is the modulation current of the VCSEL, and the system clock. Figure 5.5 shows the data waveform at the test point 3, which is the output signal from the PECL-to-TTL translator, and the system clock. It should be noted that data pattern flows correctly at all test points and logic levels are sufficient for next devices. Thus compatibility is proved by the correct execution of the data transaction.

6. CONCLUSION

As a preliminary experiment, we show the feasibility of board-to-board level substrate-guided wave optoelectronic interconnections in the real electrical system. First, we introduce a new architecture – centralized optical backplane – for board-to-board level interconnections. Second, the optoelectronic data channel is constructed compatible with standard PECL and capable of operating at 1.25 Gbps. Finally, it is employed to replace the conventional electrical data channel in a microprocessor system. Running a simple program on this system demonstrator proves compatibility. The centralized optical backplane introduced herein is for general purpose and transparent to higher layers of the system as long as appropriate protocols for media access and data transaction are provided. This technology shall provide us with an open solution for existing and future high performance systems.

7. ACKNOWLEDGEMENTS

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8. REFERENCE

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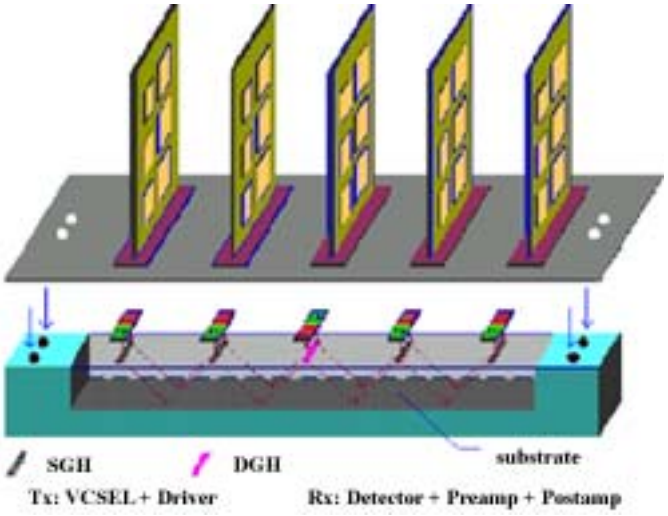
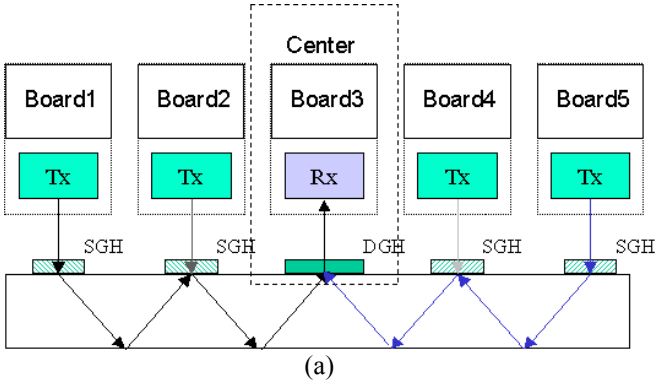
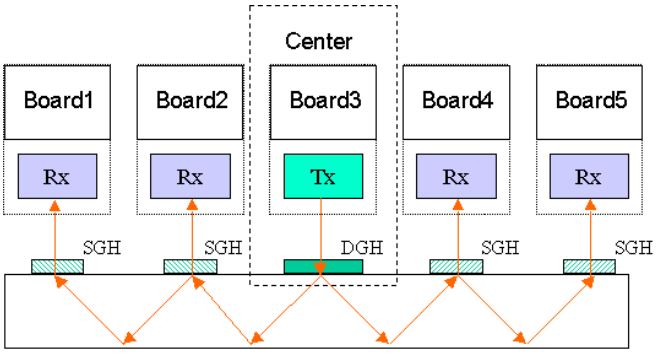


Fig 2.1 schematic diagram of centralized optical backplane



(a)



(b)

Fig 2.2 optical signal path, (a) signal delivery, and (b) signal broadcasting

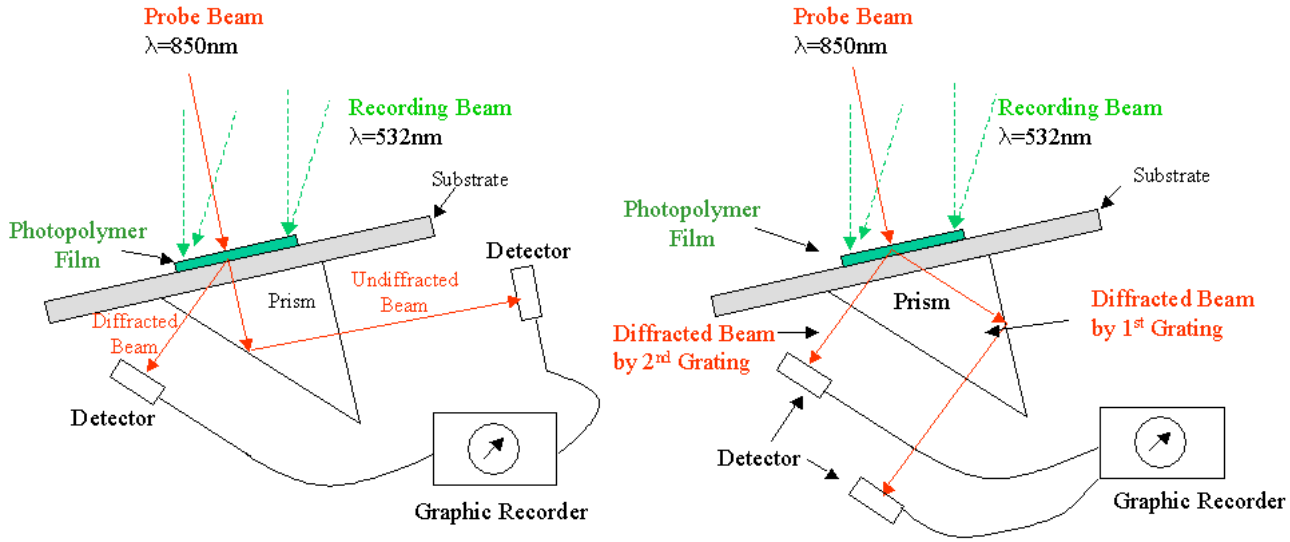


Fig 3.1 set up for (a) single grating hologram recording, and (b) double grating hologram recording

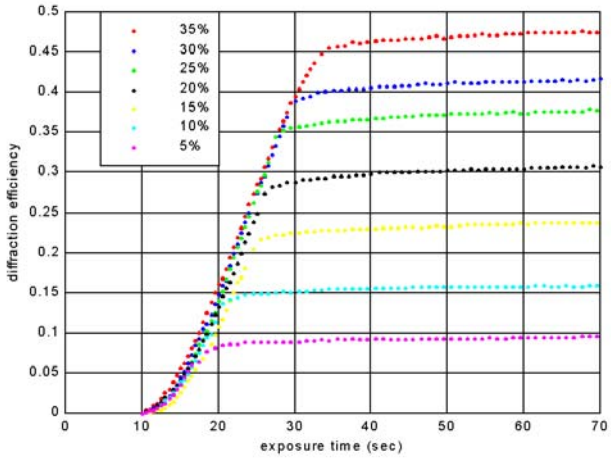
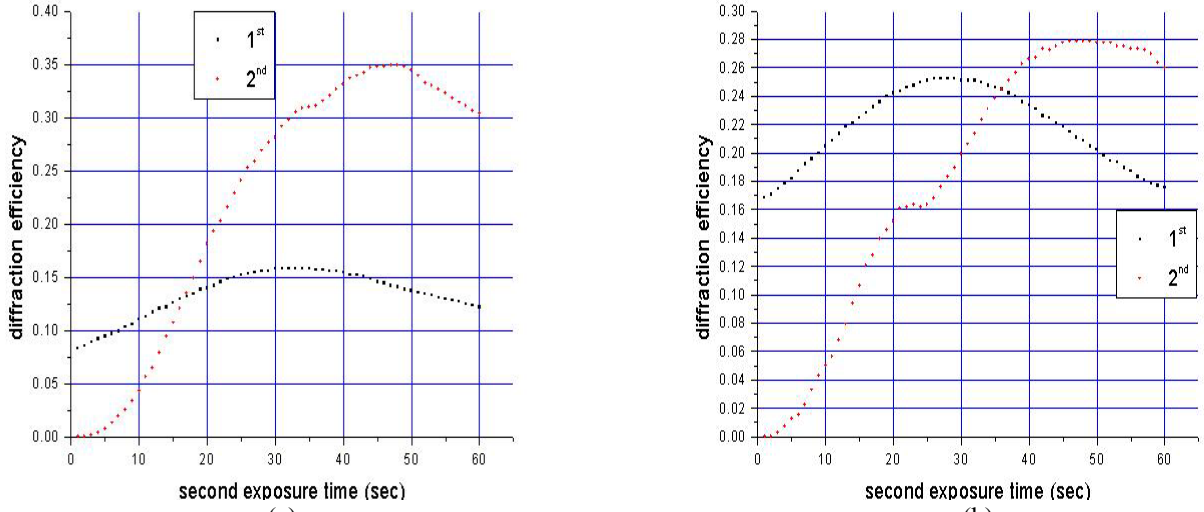
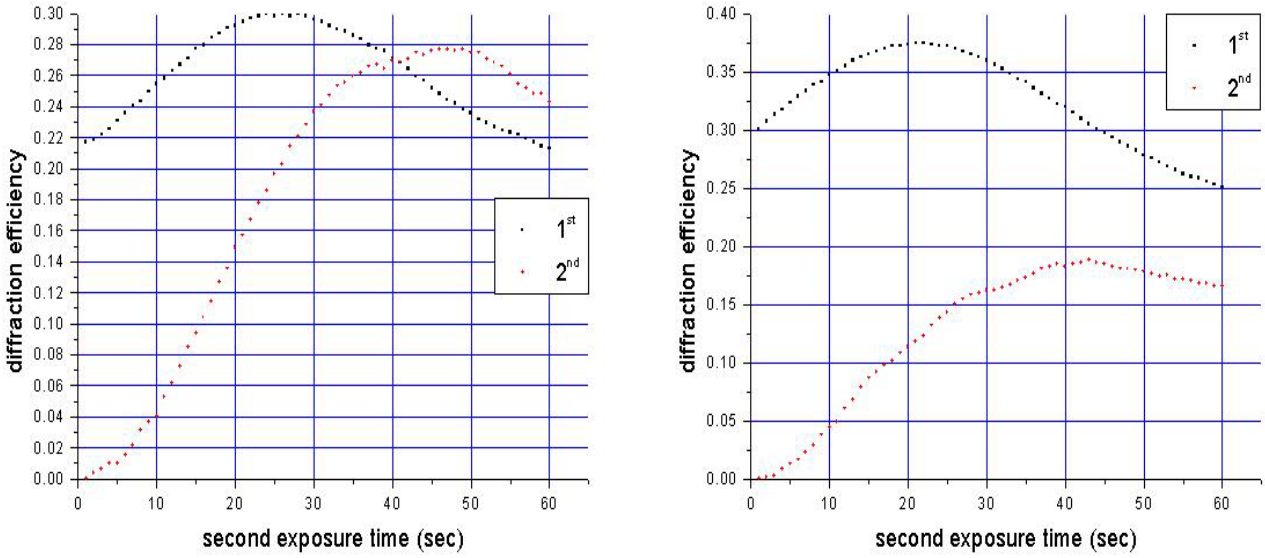


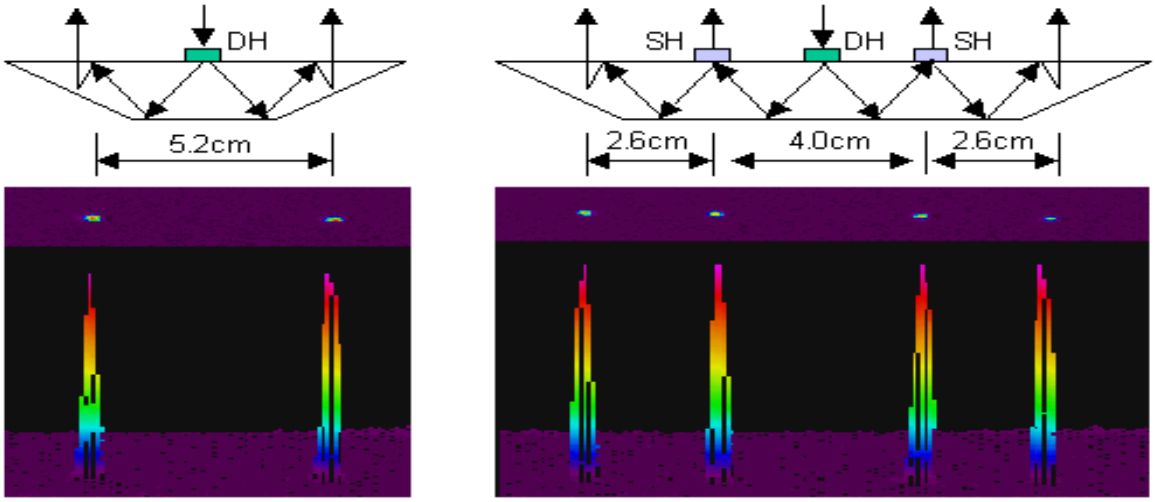
Fig 3.2 dynamic characteristics of single grating holograms





(c) (d)

Fig 3.3 dynamic characteristics of double grating holograms, the second exposure begins with (a) 6%, (b) 16%, (c) 21%, and (d) 30% diffraction efficiency in the first grating.



(a) (b)

Figure 3.4 even fan-out from the centralized optical backplane with (a) three boards, and (b) five boards

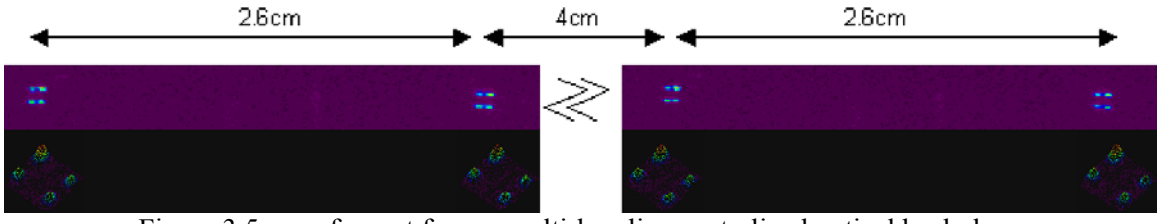


Figure 3.5 even fan-out from a multi-bus-line centralized optical backplane

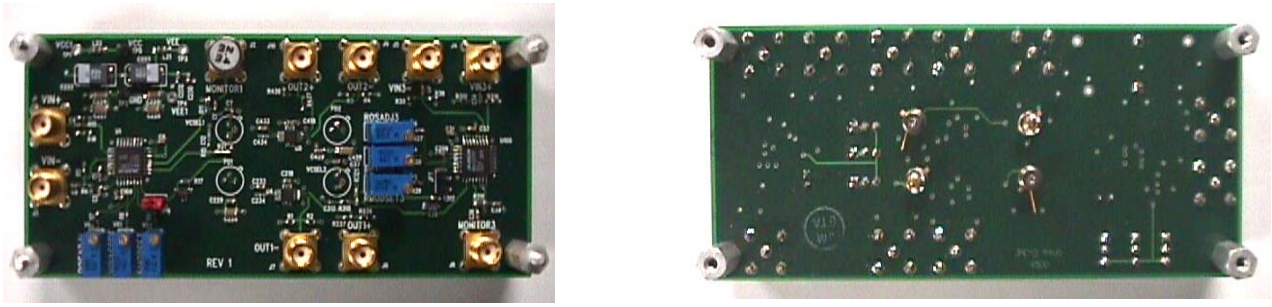


Fig 4.1 active optoelectronic module (a) front side, (b) back side

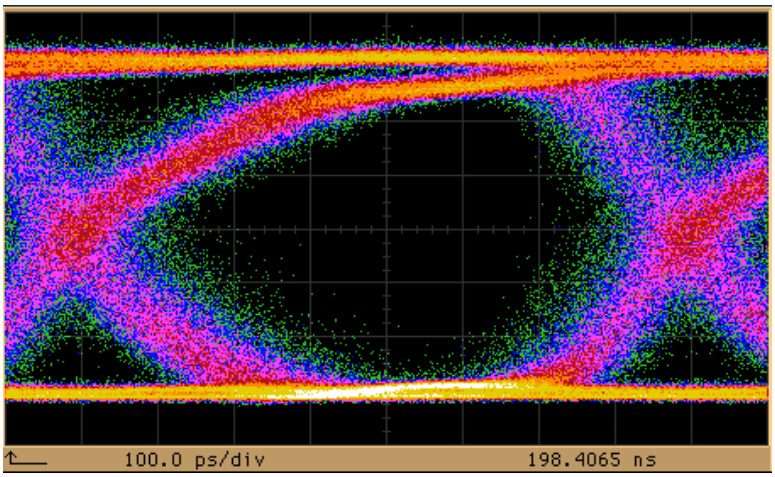


Fig 4.2 eye diagram at data rate of 1.25 Gbps

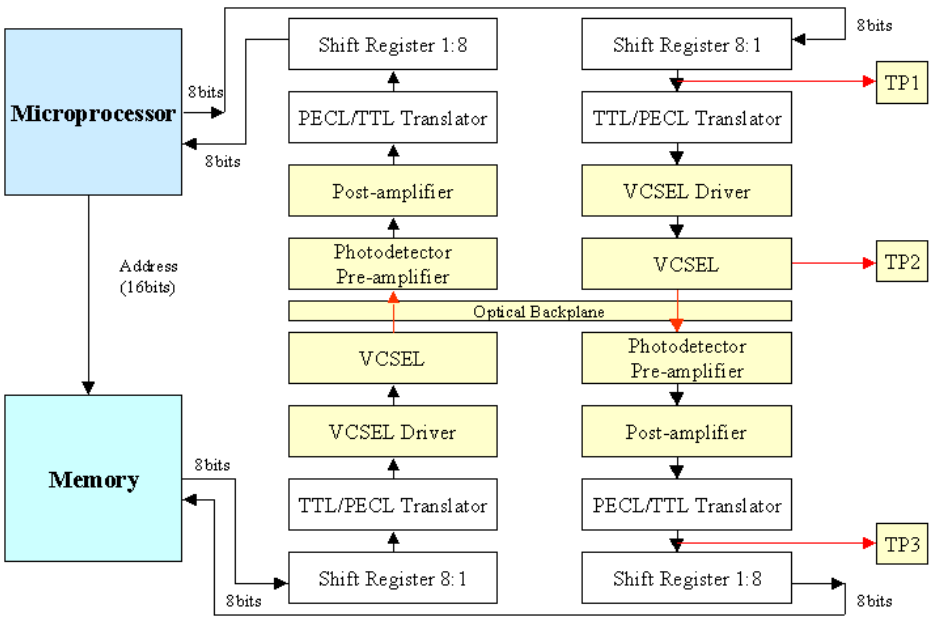


Fig 5.1 block diagram of the microprocessor system

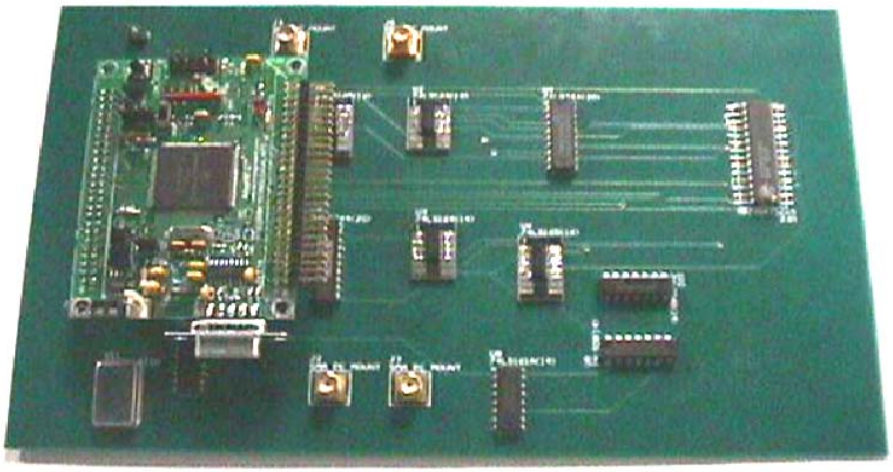


Fig 5.2 microprocessor system

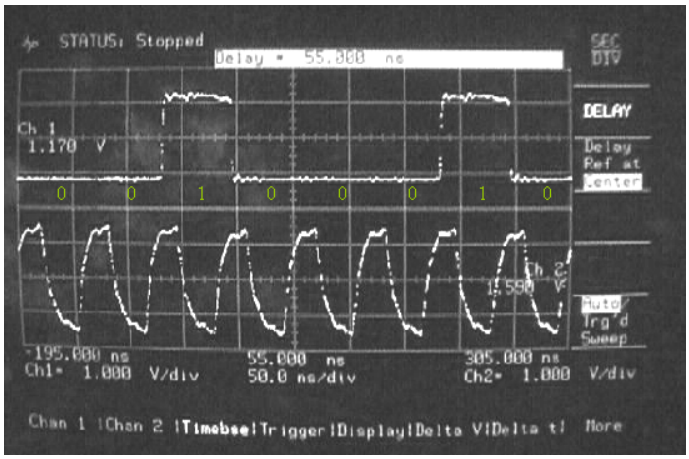


Fig 5.3 data waveform at test point 1 and the system clock

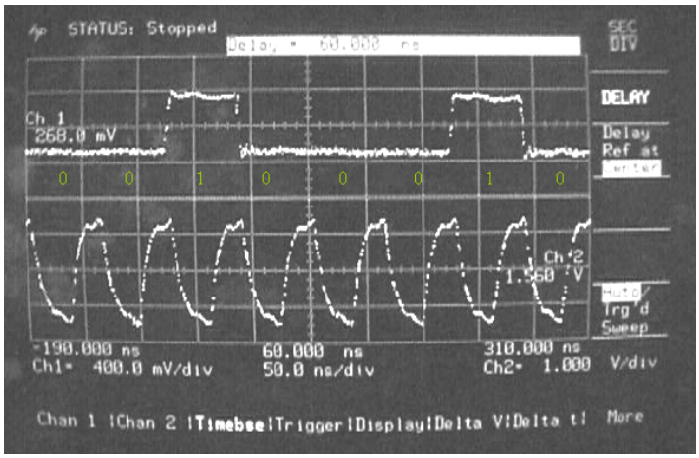


Fig 5.4 data waveform at test point 2 and the system clock

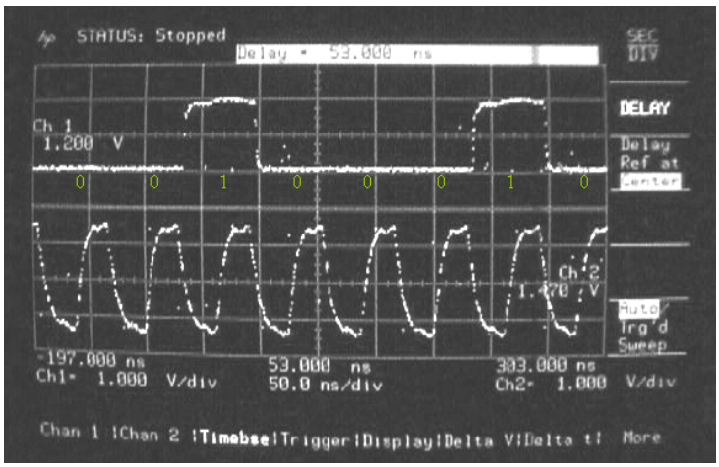


Fig 5.5 data waveform at test point 3 and the system clock