1-to-42 optoelectronic interconnection for intra-multichip-module clock signal distribution

Suning Tang and Ray T. Chen
Microelectronics Research Center, Department of Electrical and Computer Engineering, University of Texas, Austin, Texas 78712-1084

(Received 10 January 1994; accepted for publication 1 April 1994)

In this paper, we present a miniaturized compact three-dimensional optical fan-out interconnect suitable for wafer scale very large scale integrated multichip-module optical clock signal distribution. The demonstrated device employs a thin light-guiding substrate in conjunction with a two-dimensional (2D) optical hologram array. The parallel feature among fan-out beams and the planar compact structure convert the unsolvable three spatial and three angular multiple alignment problem into a single-step 2D planar one, which greatly enhances the packaging reliability. A new design scheme for reducing throughput power nonuniformity is presented for the first time. A 25 GHz 1-to-42 highly parallel fan-out interconnect was demonstrated with a signal to noise ratio of 10 dB.

The speed and complexity of integrated circuits are increasing rapidly as integrated circuit technology advances from very large scale integrated (VLSI) circuits to ultralarge scale integrated circuits. As the number of components per chip, the modulation speed, and the degree of integration continues to increase, electrical interconnections are facing their fundamental bottlenecks, such as speed, packaging, fan-out, and power dissipation. Multichip module (MCM) technology is employed to provide higher clock speeds and circuits densities.[1,2] But the state-of-the-art electrical interconnection and packaging technologies still fail to provide the required clock speeds and communication distances in intra-MCM and inter-MCM hierarchies.[3–5] High-speed massive fan-out optical interconects outperform electrical interconnects in these interconnection scenarios.[3–9] For clock signal distribution in MCMs, a successful interconnect should employ little real estate of the semiconductor wafer surface that has already been intensively occupied by electronic devices.[1,2] An array of novel optical interconnects using substrate guided wave and/or free-space, in conjunction with holographic elements, have been proposed and then reported by earlier researchers,[10–13] which may satisfy the above requirements for clock signal distribution in MCM.

In this paper, we present the demonstration of a unique three-dimensional (3D) free-space compact optical parallel fan-out interconnect for massive clock signal distribution in MCM. Unlike the previously proposed work,[9–14] an integrated wafer scale optical interconnect with 1-to-42 (6×7) parallel fan-outs is realized, using a thin light-guiding substrate in conjunction with a 2D optical hologram array fabricated on its surface. More importantly, the parallel feature among fan-out beams and the planar compact device structure convert the unsolvable three spatial and three angular multiple alignment problem into a single-step 2D planar one. The device demonstrated herein minimizes the employment of real estate of the semiconductor surface. Better device architecture is presented to increase fan-out and to improve the intensity uniformity among optical fan-out beams compared with our previous work.[15] A 25 GHz integrated 1-to-42 highly parallel optical fan-out interconnect is demonstrated experimentally in this paper. Such a device is pivotal for minaturized massive fan-out interconnect systems using planar integration technology. The demonstrated device can be fabricated by using techniques originally developed for manufacturing VLSI semiconductor circuits.

The schematic of the optical interconnect presented is shown in Fig. 1. It consists of a thin glass substrate in conjunction with a 2D hologram array fabricated on its surface. These holograms can also be fabricated directly on the semiconductor substrate surface using standard VLSI fabrication technologies. For demonstration purposes, the 2D hologram array is made out of a thin dichromated gelatin film coated on a thin glass surface. The thin glass is employed as a light-guiding plate. The hologram array consists of holograms of h_0,h_n, and multiplexed holograms of h_{mn}. The h_0 is the input coupler designed to couple the surface normal input laser beam into a substrate guided beam with bouncing angle θ_m. The multiplexed h_{mn}, having two gratings h_{mn1} and h_{mn2}. h_{mn1} is designed to fan-out the input substrate guiding beam into a linear array of surface normal fan-out beams with coupling efficiency η_{mn1}. h_{mn2} with coupling efficiency η_{mn2} is designed to deflect the substrate guiding beam into a linear array of substrate guided beams with bouncing angle θ_n. Both θ_m and θ_n (not shown in Fig. 1) are larger than the critical angle of total internal reflection of the substrate. h_n is designed to couple the array of substrate guiding beams into a 2D array of surface normal fan-out beams with coupling efficiency η_n. As a result, highly parallel massive fan-out beams are created inside the light-guiding plate together with surface normal massive fan-out beams, which are also parallel to the input laser beam. It can be seen that any permutation can be arranged without blocking guided-wave propagation inside the light-guiding substrate, in three global routing steps: permuting through input hologram (h_0), then through deflecting hologram (h_{mn2}) and finally through output hologram (h_n).

Minimization of the throughput nonuniformity of fan-out beams is an important design concern, which is determined

 0003-6951/94/64(22)/2931/3/$6.00

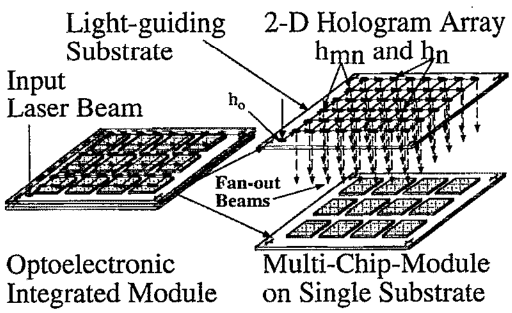

FIG. 1. Schematic of the proposed optical interconnect for MCM clock distribution.

by the arrangement of the 2D holograms and their coupling efficiencies, and of course, the number of fan-out beams as well. The methods to construct the holograms and to obtain uniform intensity among the fan-out beams were detailed in our recent publication of Refs. 8 and 15. The output power of a fan-out beam in the demonstrated device can be precisely calculated. For example, for the 1-to-42 fan-out interconnect reported herein, the output power can be written as

$$I_{m1}=I_0\eta_0\eta_{mn1}(1-\eta_{mn}-\eta_{mn2})^{m-1}, \quad (1)$$

$$I_{mn}=I_0\eta_0\eta_n(1-\eta_{mn1}-\eta_{mn2})^m(1-\eta_n)^{n-1}, \quad (2)$$

$$m=1,2,3\ldots, \quad n=2,3,4\ldots$$

where I_0 is the power of input beam, m and n stand for, respectively, the sequence of columns and rows of the 2D array of the parallel fan-out beams. As indicated by Eq. (2), a trade-off exists between the fan-out power and the grating fan-out efficiencies. Optimum values of η_m in designing a 2D hologram array with maximum throughput power for the weakest fan-out beam, corresponding to minimum power nonuniformity among fan-out beams, can be derived from Eq. (2). For example, for a 1-to-42 device with $\eta_{mn1}=\eta_{mn2}=10\%$, the optimum coupling efficiency is $\eta_n=15\%$. Note that the reflection and scattering loss is not included in Eq. (2). The diffraction efficiency of a hologram can be accurately controlled experimentally.[8,9,15] In our experiments, coupling efficiency is consistently adjustable up to 70%. The presence of each fan-out hologram can be designed and then fabricated independent. As a result, the presence of each fan-out beam can be arranged in design. The propagation loss of the glass was determined to be less than 0.1 dB/cm experimentally. Thereby, a large scale fan-out device can be provided.

Figure 2 is a photograph of surface normal 1-to-42 highly parallel optical interconnect using a glass substrate, integrated with a 2D multiplexed hologram array. The holograms were fabricated at a working wavelength of 632.8 nm, where $\eta_0=70\%$, $\eta_{mn1}=\eta_{mn1}=10\%$ and $\eta_n=19\%$ were experimentally confirmed. In this photograph, a surface normal free-space HeNe laser beam (9 mW) is coupled into the glass substrate through the surface normal input hologram η_0. The parallel fan-out beams are generated by the 2D hologram array either propagating along the substrate or normally coupling out off the substrate. The far-field pattern of the 42 surface normal fan-out beams is also displayed in Fig. 2. Variation of the 42 fan-out beams is within 12 dB, which is 13 dB better than the previous result. Note that the mode dots preserve the azimuth symmetry of the TEM_{00} beam of the input laser. As a result, coupling to a 2D photodetector array will be much easier when compared with the conventional single-mode guided wave devices.

In designing the massively parallel optical fan-out interconnect shown in Fig. 1, the fan-out packing density is another important parameter of system performance. The fan-out packing density is determined by the substrate thickness, substrate guided beam bouncing angles θ_n and θ_m, as well as the angle α between the two projection of holographic grating vector of h_0 and h_{mn2} on the surface of a glass substrate. In our experiment we selected $\alpha=90°$ and set $\theta_n=\theta_m=\theta_d=45°$ for symmetric purpose. Therefore, the separation between any two nearest fan-out beams is given by

$$s=(2t)\tan(\theta_d), \quad (3)$$

where t is the thickness of the glass substrate. By selecting the glass thickness and/or coupling angles, the desired packing density of fan-out beams can be obtained. The location of the fan-out beams can be easily determined as $(x_m,y_n)=(ms,ns)$, where $m,n,=1,2,3\ldots$.

The input beam angular misalignment will also cause a spatial shift of the fan-out beam due to the shift of diffraction angle θ_d within the substrate. Based on the phase-matching condition, we have

$$n_s\sin(\theta_d)=\lambda/\Lambda_x-\sin(\theta_i) \quad (4)$$

where Λ_x is the surface grating period, n_s is the substrate index, θ_d is the diffraction angle, and θ_i is the incident angle of the input laser beam. Differentiating Eq. (4) while holding λ fixed, we obtain

$$d\theta_d=-[\cos(\theta_i)/(n_s\cos(\theta_d)]\,d\,\theta_i. \quad (5)$$

The resulting maximum amount of spatial shift ΔL can be determined based on Eqs. (3) and (5), which is

$$\Delta L=2t[\tan(\theta_d)-\tan(\theta_d\pm d\theta_d)]. \quad (6)$$

For the device demonstrated herein with $t=3.0$ mm, $\theta_i=0°$

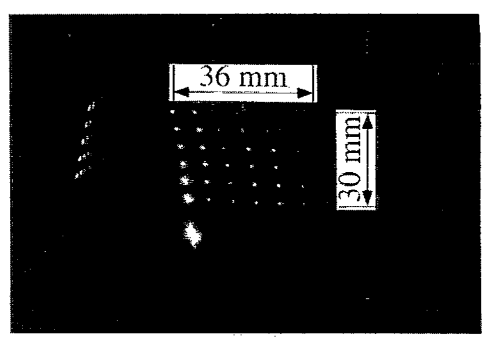

FIG. 2. Photograph of a surface normal 1-to-42 highly parallel optical fan-out interconnect. The far-field pattern of fan-out beams is also shown.

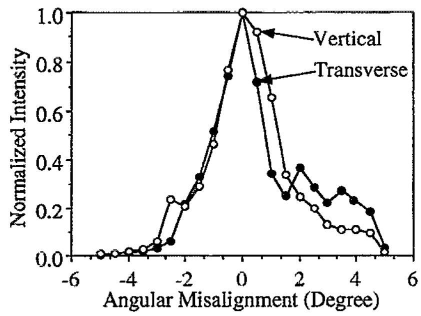

FIG. 3. Experimental results of fan-out efficiency vs angular misalignment of the input beam. The two rotational axes are perpendicular to each other and perpendicular to the input beam as well.

and θ_d=45°, 0.5°, and 0.05°, input angular misalignments correspond to ~100 μm and ~1 μm spatial shifts, respectively. Equation (6) indicates that the unsolvable problem of the three spatial and three angular multiple alignments is converted into a single-step 2D planar one. Standard state-of-the-art 2D planar alignment techniques, with the resolution of ~0.1 μm developed for fabricating VLSI circuits, can be employed to integrate the demonstrated device to a Si/VLSI multichip module. Figure 3 shows the experimental results of the diffraction efficiency of the fan-out beam (m=3, n=3) versus input angular misalignments of the device shown in FIg. 2. The angular full width at half maximum of the diffraction efficiency is determined to be about ±1°.

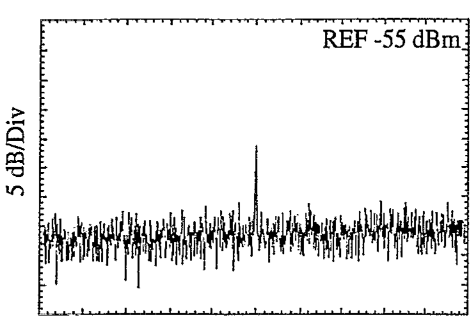

FIG. 4. 25 GHz optical beating signal through the optical fan-out interconnect shown in Fig. 2, obtained from the weakest fan-out beam (m=6, n=7).

An optical coherent beating signal was employed as the optical clock signal.[16] By colinearly propagating two single longitudinal laser beams (HeNe laser of λ_1=632.80 nm and dye laser of λ_2=~632.83 nm) through the 1-to-42 fan-out interconnects fabricated, a beat signal equivalent to an optical wave modulated at a microwave frequency of 25 GHz, was detected at the weakest fan-out (6,7) and the result is shown in Fig. 4. A signal-to-noise ratio (SNR) of 10 dB is observed. The SNRs of the 42 beams were measured independently. The result shown in Fig. 4 represents the worst case.

In summary, we represent the first effort to construct a 3D integrated free-space compact optical fan-out interconnect for wafer scale fast clock signal distribution. The power uniformity among fan-out beams, the number of fan-out were significantly improved through better design of 2D holograms, compared with our previous work.[15] It was shown that the difficulties associated with the complicated 3D multiple alignments are significantly reduced through the parallelism among the fan-out beams and the unique planar device feature. 25 GHz clock signal distribution was demonstrated experimentally for the first time with 42 parallel fan-outs.

This research is sponsored by Cray Research Inc., Novex Corporation, Physical Optics Corporation, the Army Research Office, and the University of Texas at Austin.

[1] D. P. Seraphim and D. E. Barr, Proc. SPIE, **1390**, 39 (1990).
[2] C. Neugerbauer, R. O. Carlson, R. A. Fillion, and T. R. Haller, in *Multichip Modules, Compendium of 1989 Papers* (International Electronic Packaging Society, 1989) pp. 149–163.
[3] J. W. Goodman, F. I. Leonberger, S. Y. Kung, and R. A. Athale, Proc. IEEE **72**, 850 (1984).
[4] M. R. Feldman, S. C. Esener, C. C. Guest, and S. H. Lee, Appl. Opt. **27**, 1742 (1988).
[5] F. E. Kiamilev, P. Marchand, A. V. Krishnamoorthy, S. C. Esener, and S. H. Lee, IEEE J. Light Technol. **9**, 1674 (1993).
[6] S. Tang, R. T. Chen, and M. Peskin, Opt. Eng. (to be published).
[7] R. T. Chen, S. Tang, T. Jannson, and J. Jannson, Appl. Phys. Lett. **63**, 1032 (1993).
[8] R. T. Chen, S. Tang, M. M. Li, D. Gerald and S. Natarajan, Appl. Phys. Lett. **63**, 1883 (1993).
[9] R. T. Chen, H. Lu, D. Robinson, M. Wang, G. Savant, and T. Jannson, IEEE J. Light Technol. **10**, 888 (1992).
[10] P. Cinato and K. C. Young, Jr., Opt. Eng. **32**, 852 (1993).
[11] R. K. Kostuk, J. W. Goodman, and L. Hesselink, Appl. Opt. **26**, 3947 (1987).
[12] K. Pastani and W. M. Hubbard, Appl. Opt. **31**, 4863 (1992).
[13] M. R. Feldman, Proc. SPIE **1390**, 427 (1990).
[14] M. R. Feldman and C. C. Guest, Opt. Eng. **28**, 915 (1989).
[15] S. Tang and R. T. Chen, SOA/IEEE Integrated Photon. Research, Technical Digest Series, Vol. 3, pp. 277–279, 1994; S. Tang and R. T. Chen, IEEE Photon Technol. Lett. **6**, 299 (1994).
[16] R. T. Chen, H. Lu, D. Robinson, Z. Sun, T. Jannson, D. V. Plant, and H. R. Fetterman, Appl. Phys. Lett. **60**, 1883 (1992).