The Integration of CMOS Process-compatible Optoelectronic Interconnects for High-speed Communications

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ABSTRACT

The design and integration of a fully embedded Si-CMOS process-compatible optical interconnects are presented. The transmitting and receiving functions will be incorporated within the embedded optoelectronic interconnection layers of 3-D integrated multilayer boards and ASICs. All elements including waveguide, coupler, detector and laser for the fully embedded board-level optical interconnection system are developed. The propagation loss of waveguide is 0.58dB/cm at 632.8nm and 0.21dB/cm at 850nm. The 45-degree TIR (total internal reflection) micro-mirror couplers with high coupling efficiencies are formed by reactive ion etching. The MSM (metal-semiconductor-metal) photo-detector array is fabricated on a GaAs wafer by a CMOS compatible technique. The external quantum efficiency of 0.4A/W and 3dB bandwidth of the integrated MSM photo-detector of 2.648GHz are experimentally confirmed. The VCSEL array with a sacrificial layer for the epitaxial liftoff of VCSEL from the GaAs substrate is designed and manufactured. A 1x12 array of VCSELs, MSM photo-detectors and polyimide channel waveguides via 45-degree TIR micro-couplers are integrated on Si wafer. The experimental performances of the highly integrated system are given.

Keywords: optoelectronic interconnect, polymeric waveguide, micro-mirror, MSM photo-detector, VCSEL

1 INTRODUCTION

The trend to higher data rates per microprocessor, and the rapidly increasing number of microprocessors per machine, results in much higher speed internal buses and external access. The Semiconductor Industry Association (SIA) roadmap for CMOS technology predicts that by the year 2009 more than 5000 chip I/O (pads) will be required and off chip (chip-to-board) clock rates will reach 2-3 GHz.[1] Conventional electrical interconnects are unable to offer this high frequency and wide-band performance due to poor isolation at frequencies greater than a few GHz. Furthermore, it is extremely difficult for multiprocessor computing systems involving a large number of fan-outs and long interconnection lengths (>15cm) to obtain synchronous high-speed (>500MHz) clock distribution using electrical interconnections,[2] so the system performance may be limited more and more severely by electrical interconnections. Optical interconnect can be used to break these bottlenecks in high-speed communications.[3] Its potential advantages include large bandwidth, no capacitive loading, higher maximum practical frequency, smaller minimum number of layers needed for high-performance

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interconnection, higher interconnect density, immunity from electromagnetic interference (EMI) and no crosstalk.[4] Thus the future of computer system communication will benefit form it.

Basically, there are various types of optical interconnect suitable for optical backplane applications such as optical fiber, free space interconnects, and polymer waveguides.[5-7] The low packing density and topology incompatibility with printed circuit boards (PCB) of optical fibers limit their use in backplane and board-level applications. Free space optical interconnections are very popular and offer extremely high interconnect density and low crosstalk, however, complexity of alignment and intolerance of dust particles are their inherent problems. Therefore, polymeric channel waveguides are thought to be best suited for optical backplane and board-level interconnects. Compared to free space optical interconnects, guided wave optical interconnects achieve higher package density, have an easier fabrication process and offer more relief for alignment of different components than free-space optical interconnects.

This project aims to solve the packing-compatible problem by a fully embedded board-level optoelectric interconnection system, which could provide high-speed optical communication within one board. All the components, including waveguide, coupler, detector and laser, which are vital to the realization of this fully embedded board-level optoelectronic interconnects have been developed and fabricated on the VLSI scale.

2 SYSTEM PROTOTYPE

The schematic of a fully embedded optoelectronic interconnection is presented in Fig.1, where the optoelectronic interconnect layer is sandwiched between several electrical interconnect layers. The main parts of the optoelectronic interconnect system include the thin film metal-semiconductor-metal (MSM) photo-detector, the thin film vertical cavity surface emitting laser (VCSEL) and the multi-mode polyimide waveguide with a 45^o micro-coupler. Within the optoelectronic interconnect layer, pulsed laser light from the VCSEL is coupled into the multi-mode waveguide through a 45^o totally internal reflection (TIR) micro-coupler. It propagates through the waveguide to the destination, there it is reflected by another 45^o TIR micro-coupler, and finally it illuminates vertically on the active area of the photodetector. The light signal detected by the photodetector is then converted to an electrical signal and sent to the receiving IC. The driving electrical signal to modulate the VCSEL and the demodulated signal received by the photoreceiver are all through electrical vias connecting to the PC board surface, where the driving circuit for VCSEL and amplifying circuit for photodetector are located. In this way, all the opto-electronic parts are buried under layers of PC board. The buried opto-electronic parts provide the performance improvement without occupying the surface of PC-board or interfering with the function of the electrical parts.

3 VERTICAL CAVITY SURFACE EMITTING LASER (VCSEL)

The vertical cavity surface emitting laser (VCSEL) was selected as the light source due to its advantage in electron-optical integration, its very thin laser cavity and surface-normal

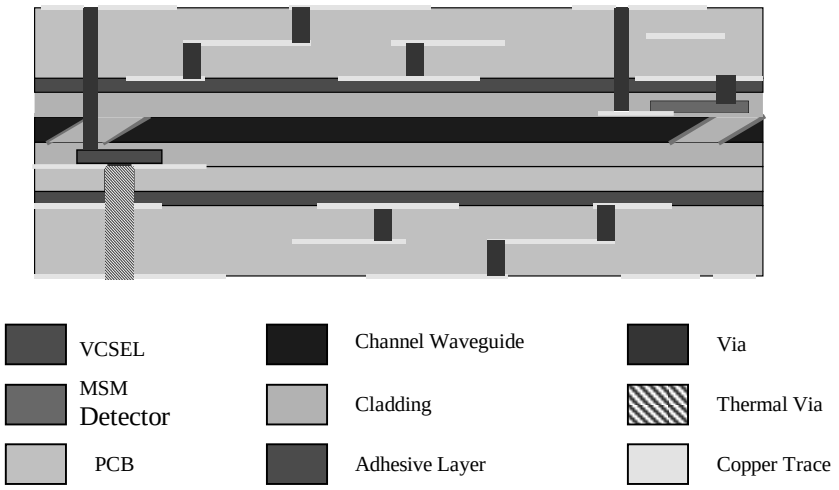


Fig.1 Schematic of a fully embedded optoelectronic interconnection

emitting characteristic. The VCSEL wafer contains four major epitaxially grown layers: a thin sacrificial layer, bottom n-DBR (Distributed Brag Reflector), active layer and top p-DBR, as shown in Fig. 2. The 40nm thick $Al_{0.9}Ga_{0.1}As$ sacrificial layer, which was used for the liftoff of thin film VCSELs, was fabricated on top of the GaAs substrate. The bottom n-DBR was composed of 32.5pairs of $Al_{0.9}Ga_{0.1}As$/ $Al_{0.15}Ga_{0.85}As$ quarter wave stacks. To yield lower resistance of the n-DBRs, linear grade composition layer was inserted between the $Al_{0.9}Ga_{0.1}As$/$Al_{0.15}Ga_{0.85}As$ layer. Three GaAs quantum wells were formed within the active region and the optical thickness of active region was designed to emit an 850nm laser. The top p-DBRs was composed of 23 pairs of $Al_{0.9}Ga_{0.1}As$/ $Al_{0.15}Ga_{0.85}As$ layer.

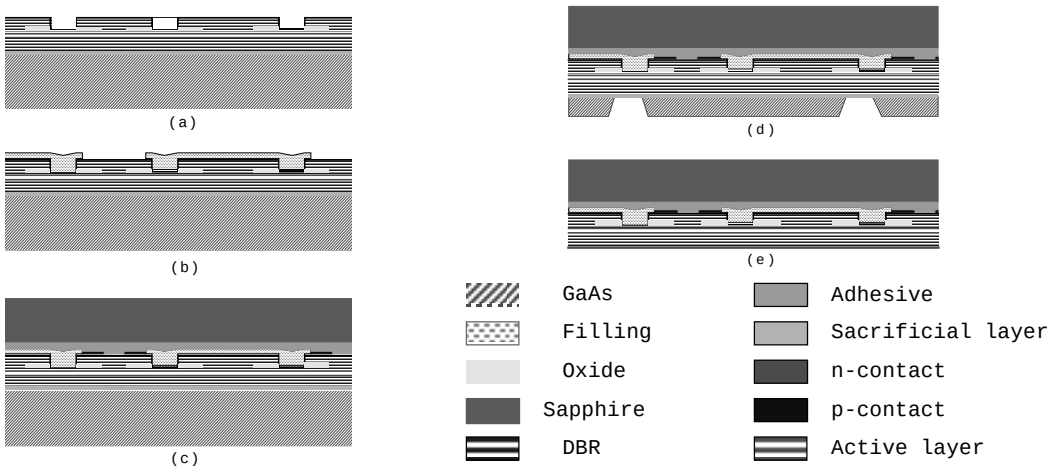


Fig.2 Thin VCSEL fabrication process

The donut shaped trenches are used to define each VCSEL region and current confinement through lateral oxidation, as shown in Fig.2(a). The designed depth of the trench is 2.99μm. Etching must be stopped just above the active layer, so precise control of depth is required. Non-selective $H_2SO_4/H_2O_2/H_2O$ based etchant was used to etch the trenches. The etched trench was filled with spin on glass (Fig. 2(b)) before the thinning of the VCSEL. Without this filling, VCSEL would be very fragile after thinning.

The initial thickness of the VCSEL array with the GaAs substrate was 250μm. To integrate the VCSELs with the waveguide array, the VCSEL array has to be thin enough. That is, the GaAs substrate needs to be removed. There are two methods to make thin VCSEL: chemical mechanical polishing (CMP) and epitaxial liftoff. [8,9] The substrate removal began with CMP and was followed by epitaxial liftoff. The epitaxial liftoff method is based on the extremely selective etching of AlAs compared with GaAs in dilute hydrofluoric acid. A 40nm epitaxially grown $Al_{0.9}Ga_{0.1}As$ thin layer is inserted between the GaAs substrate and the bottom n-DBR as a sacrificial layer in the epitaxial liftoff. The VCSEL was bonded to a large flat sapphire substrate using Crystal Bond for the purpose of easy handling and even polishing(Figure 2(c)).

First, the thick VCSEL was thinned down to 50μm using 2μm grain size aluminum oxide powder and then down to 42μm by polishing with 0.5μm and 0.1μm powder. The epitaxial liftoff method was then used to get rid of the remaining substrate. The epitaxial liftoff to doff the GaAs substrate of the VCSEL is relatively tricky because DBR layers have the same composition material as the sacrificial layer. Top down etching will cause damage to DBR. To avoid this problem, a hole in the GaAs substrate backside was formed using GaAs selective etchant (Figure 2(d)). The etchant was introduced through this hole to etch the sacrificial layer. The high selective etchant was composed of citric acid monohydrate, potassium citrate and hydrogen peroxide. The estimated etch rate of this system was 223nm per minute and the selectivity was over 1000 for $Al_{0.9}Ga_{0.1}As$ and GaAs structure. Finally, a VCSEL array of about 8μm thick has been obtained (Figure 2(e)).

The reflectance as a function of wavelength of the DBR is shown in Fig.3. It can be seen that the bandwidth of the reflectance of the DBR is 86.5nm and Fabry-Perot dip is located at 854nm.

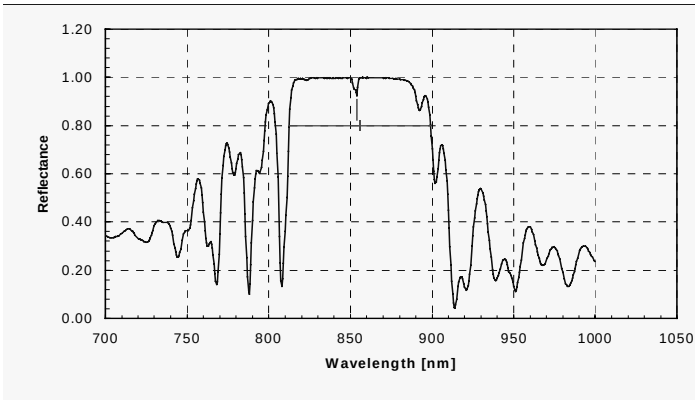
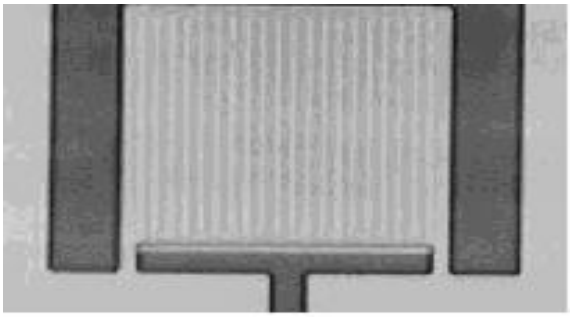


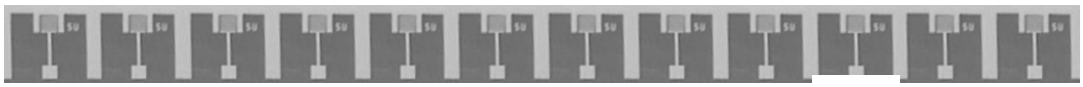
Fig.3 Reflectance as a function of wavelength of the DBR

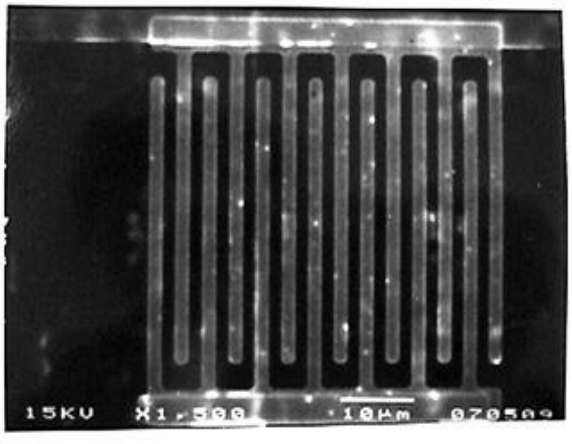
The electrical and optical characteristics of the VCSEL before and after thinning were measured and compared. The results indicated that there was no degradation in electrical and optical characteristics after the mechanical removal of substrate. The threshold voltage is greatly reduced from 1.5V to 1.0V after thinning. This result comes from reducing the resistive GaAs substrate thickness. There is little change of laser output power before and after thinning.

4 MSM PHOTO-DETECTOR

We chose the metal-semiconductor-metal (MSM) photodetector as the receiver for the fully embedded board-level optoelectronic interconnect system because it can provide a very high demodulate speed due to the fast transit time of electron and hole pairs and is compatible with Si CMOS fabrication procedure. [10,11]







The structure of a 1x12 thin film MSM photodetector array that can be directly integrated onto the system architecture is shown in Fig. 4. The photodetector was fabricated on the