Polymer Waveguide based Fully Embedded Board Level Optoelectronic Interconnects

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Abstract

A fully embedded board-level guided wave optical interconnection is presented to solve the packaging compatibility problem. All elements involved in providing high speed optical communications within a board are demonstrated. Experimental results on a 12-channel linear array of polymeric waveguides, thin film VCSELs (10 μm), and GaAs MSM photodetectors suitable for a fully embedded implementation are provided. By embedded approach, all the real estate of the PC board surface are occupied by electronics so that one only observes the performance enhancement due to the employment of optical interconnection without any interface problems between electronic and optoelectronic components. Thin film 1X12 linear array VCSEL and GaAs MSM detector were demonstrated and thermal management issue of the VCSEL in the fully embedded scheme was disscussed.

1. Introduction

The speed and complexity of integrated circuits are increased rapidly as integrated circuit technology advances from very large scale integrated (VLSI) circuits to ultra large scale integrated (ULSI) circuits. As the number of devices per chip, the number of chips per board, the modulation speed and the degree of integration continue to increase, electrical interconnects are facing their fundamental bottle-necks, such as speed, packaging, fanout, and power dissipation. Multichip module (MCM) technology is employed to provide higher data transfer rates and circuit densities [1,2]. The employment of copper and lower dielectric constant materials can release the bottleneck in a chip level for next several years. However, the interconnection roadmap published by Sematech still predicts a major bottleneck by 2006 [3]. The employment of optical interconnects will be one of the major alternatives for upgrading the interconnection speed whenever conventional electrical interconnection fails to provide the required bandwidth.

Machine to machine interconnection has already been significantly replaced by optical means. The major research thrusts in optical interconnection are in the backplane and board level where the interconnection distance, the associated parasitic RLC effects and the large fanout induced impedance mismatch are to jeopardize the bandwidth requirements. Optical interconnection has been widely agreed as a better alternative to upgrade the system performance. A fully embedded board-level guided wave optical interconnection is presented in Figure 1, where all elements involved in providing high speed optical communications within one board are shown. These include a vertical cavity surface emitting laser (VCSEL), surface-normal waveguide couplers, and a Polyimide-based channel waveguide functioning as the physical layer of optical bus and a photoreceiver. The driving electrical signal to modulate the VCSEL and the demodulated signal received at the photoreceiver are all through electrical vias connecting to the surface of the PC board. The fully embedded structure makes the insertion of optoelectronic components into microelectronic systems much more realistic when considering the fact that the major stumbling block for implementing optical interconnection onto high performance microelectronics is the packaging

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incompatibility.

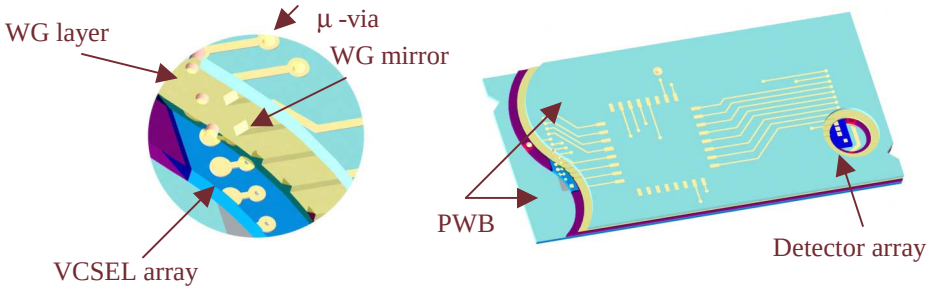
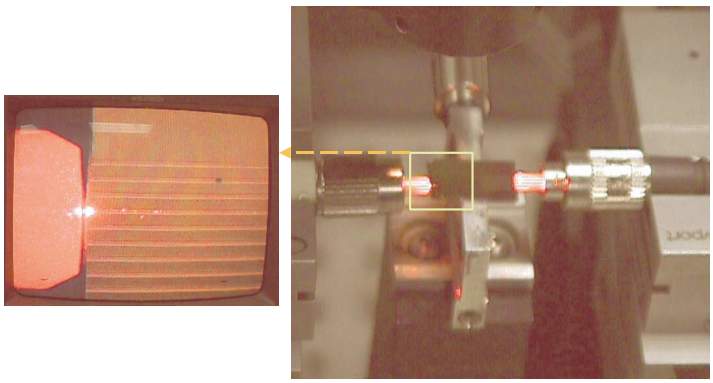


Figure 1. Schematic diagram of the fully embedded PWB level optical interconnects

2. Polymer Waveguides and 45° waveguide mirror

To provide system integration using guided wave optical interconnection, polymer-based material has its exclusive advantages. It can be spin-coated on a myriad of substrates with a relatively large interconnection distance. To ensure the desired electrical and mechanical properties imposed on board level optical interconnection, and to meet the required optical properties for the low loss waveguide formation, the photosensitive polyimide provided by Amoco Chemicals was used for the waveguide fabrication. 45° total internal reflection(TIR) mirrors were fabricated by oblique reactive ion etching(RIE) to provide surface normal coupling. The propagation loss of the TE mode of the channel waveguide is 0.21 dB/cm at 850 nm.

The crosstalk of parallel channel waveguides is important factor in communication. Our channel waveguide pitch is 250μm and the width of waveguide is 50μm. The refractive difference between core and cladding is about 0.01. To measure crosstalk, the sample was put on auto-aligner and the fiber coupled laser light with wavelength of 630nm was lunched into one channel among the waveguides. The output of the signal was detected from the adjacent channel from the input channel. Figure 4. shows a test setup. Figure 2(a) shows input coupling. Laser light was lunched from the end of fiber ferrule to waveguide. Figure 2(b) shows test setup. The input power at waveguide is –21 dBm and the output power of the adjacent channel is -53 dBm. The measured crosstalk was 32dB.



(a) (b)

Figure 2. Test setup for the crosstalk measurement.

3. Thin film VCSEL fabrication and thermal property of the VCSEL in the embedded integration

High performance vertical cavity surface emitting lasers (VCSELs) are commercially available with the output wavelength of 850nm. These laser devices, compared to conventional edge emitting lasers, provide a very low threshold current with much less temperature sensitivity, moderate optical power (few mW), very high direct modulation bandwidth (> 14 GHz), wide operating temperature range (-55 to +125 ºC), and ease of packaging in an array configuration due to the unique surface-normal output nature. Planar configuration of VCSELs allows these devices to be fabricated, wafer scale tested with conventional microelectronics manufacturing processes. The unique surface-normal emitting nature of the device allows us to use exactly the same packaging scheme for coupling light from VCSEL into waveguide as that used for coupling light from waveguide into photodetector.

To incorporate the VCSEL array onto the fully embedded architecture, the VCSEL array has to be thin enough to build such a 3-D structure. We fabricated oxide confined thin film linear VCSEL array. The VCSEL's epitaxial structure was grown on GaAs substrate. An etch stop layer of 100nm thick was grown and then GaAs buffer layer, 40.5 pairs of n-DBR, three GaAs quantum wells, and 23 pairs of p-DBR were grown. Total thickness of epitaxial structure is 10μm. Fabrication started with wet etching to make annular shape trench which provides isolation of each device and defines oxide confinement region. Wet oxidation was carried out in quartz tube furnace which was held at 460°C. Spin on glass(SOG) was coated on the entire wafer for electrical isolation and side wall sealing. The SOG opening process was followed for p-contact metalization. After finishing device processes, substrate removal process was followed. Devices were first mechanically thinned down to 250μm. These devices were back etched using wet etchant to make various thick VCSELs(200, 150, 100μm). Ten micrometer thick VCSEL was prepared by substrate removal technique[4],[5].

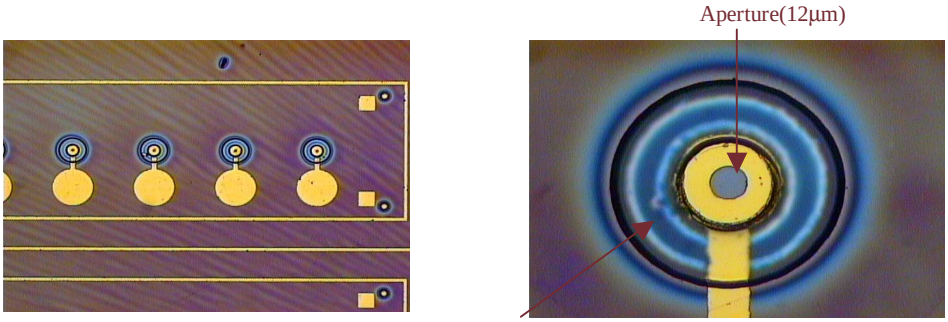


Figure 3. 1X12 linear VCSEL array and enlarged view of VCSEL

Light-current characteristic of various thickness VCSEL were measured. Threshold current were 3.5mA for all devices without showing any degradation, however slope efficiency was increased by reducing device thickness due to the reducing device thermal resistance. The substrate removed VCSEL(10μm thick) shows higher slope efficiency than thicker devices did(Figure 4). By reducing device thickness, more strate slope efficiency even high injection current level. High frequency modulation characteristics was also measured. Electrical signal was fed into device using a high frequency probe. Eye diagram operating 2.25GHz is shown in figure 5.

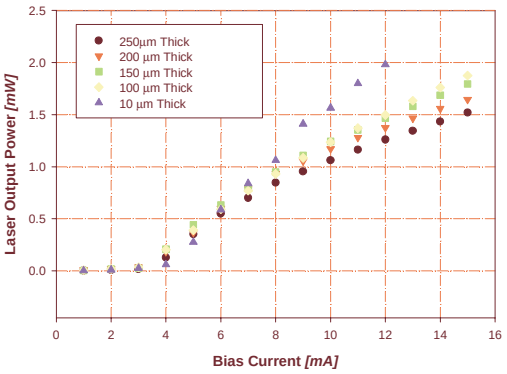


Figure 4. L-I charateristics of various thickness VCSEL

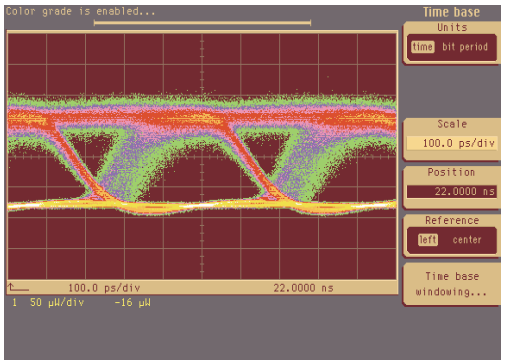


Figure 5. Modulation characteristics of theVCSEL (2.25GHz)

The VCSEL is a major heat source unlike other optical components in embedded optical interconnects structure. The embedded VCSEL arrays are thermally isolated by surrounding insulators therefore heat builds up and the operating temperature increases, eventually face with critical operating temperature. High operating temperature reduces life time of device and laser output power. Reliable operation of the VCSEL is needed for proper heat management. Remove heat efficiently is a challenging task in embedded structure because we have to consider packaging compatibility to traditional PWB process and effective and simple cooling mechanism.

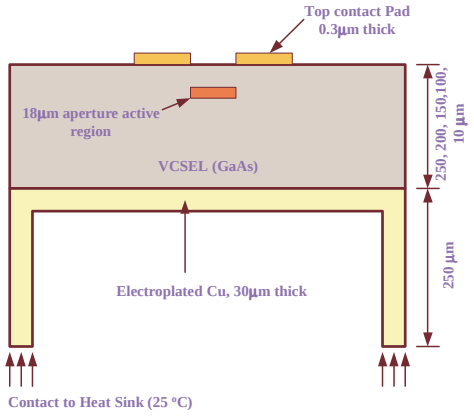


Figure 6. Thermal via structure

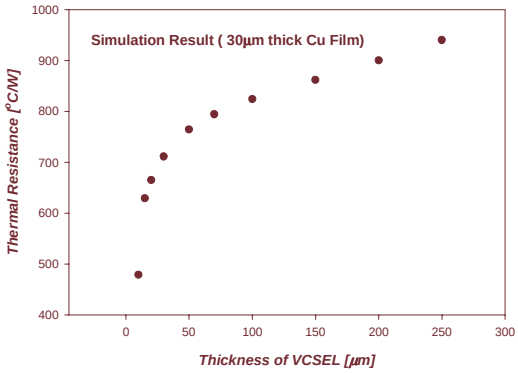


Figure 7. Thermal resistance of the VCSEL as a function of device thickness.

We introduced an effective heat management scheme. The n-contact metal affiliated with the bottom DBR mirror of the VCSEL die was directly electroplated with copper during process without any other thermal conductive paste which has lower conductivity than copper. Usually several tens of micrometer thick copper was deposited in copper contained acid chemical solution during PWB process. It can be used as a very good electrical and thermal passage simultaneously. Direct bonding of a device using electroplating reduces thermal resistance of device due to the absence of low conductivity bonding paste.

The ANSYS program was used to perform 2-D finite element thermal distribution analysis. The thermal conductivities of GaAs, DBR, copper and thermal conductivity epoxy (H20E, Epotek) are 4.6 X 10^{-5} W/μm ^{o}K, 2.3 X 10^{-5} W/μm K, 4 X 10^{-4} W/μm ^{o}K and 2.9X10^{-5} W/μm ^{o}K, respectively. We used different thermal conductivity for DBR (Distributed Bragg Reflector) and GaAs. Heat is generated due to the Bragg reflector's resistance and imperfect conversion efficiency in active region. However, the heat generated due to the DBR is relatively small compared with active region, therefore we ignored this term in simulation[7]. The heat generation rate in active region (circular shape, diameter of 18μm) is based on measured value which is 20mW per VCSEL.

The cooling structure of the device was shown in figure 6. Thirty micrometer thick electrodeposited copper film was electro-deposited on the n-contact metal of the VCSEL. We chose 30 μm thick copper film as a heat sink because this is the thickness of copper trace in electrical layer for PWB. The bottom surface of copper block is maintained at 25^{o}C.

A theoretically determined thermal resistance of various thickness VCSEL were shown in figure 7. Ten miicrometer thick VCSEL has nearly half of the thermal resistance of 250μm thick VCSEL. The substrate removed VCSEL having a total thickness of 10μm shows superior optical and thermal characteristics. We can determine maximum allowable device thickness to meet the requirement of reliable operation in the fully embedded integration.

5. Conclusion

A fully embedded board-level guided wave optical interconnection is presented. All elements involved in providing high speed optical communications within one board are demonstrated. These include a thin vertical cavity surface emitting laser (VCSEL), surface-normal waveguide couplers, a polyimide-based channel waveguide functioning as the physical layer of optical bus and a photoreceiver. The driving electrical signal to modulate the VCSEL and the demodulated signal received at the photoreceiver can be applied through electrical vias connecting to the surface of the PC board. The thermal resistance of fully embedded VCSEL in board level optical interconnect has been calculated using two dimensional finite element method and validated by comparing with measured thermal resistance. Directly electroplated copper film was verified as a simple and effective heat sink in the fully embedded structure. The substrate removed VCSEL had the lowest thermal resistance and the best quantum effciency when compared with the thicker ones out of the same wafer. Employing thin VCSEL in embedded optical interconnects provides a simple packaging strategy and releases thermal related issue.

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