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Demonstration of the centralized optical backplane architecture in a three-board microprocessor-to-memory interconnect system

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Abstract

A prototype of a novel interconnection architecture called the centralized optical backplane (COB) was experimentally demonstrated in a three-board microprocessor-to-memory interconnect system. COB keeps the advantages of bus architecture while at the same time providing uniform optical signal fan-outs. In the prototype, the required connectivity for the microprocessor-to-memory interconnect was achieved by using a COB. The optoelectronic interface modules were optimized to support high-speed processing elements at data rates up to 1.25 Gbps. This demonstration illustrates the conceptual design of the COB and its feasibility in real systems.

Keywords: Optical interconnect; Optical backplane; Optoelectronic interface

1. Introduction

The ever-increasing demand on bandwidth and the physical limitations of metal interconnect have imposed a bottleneck at the board-to-board level in the interconnect hierarchy [1]. Optical interconnect is believed to be the technology to resolve this bottleneck because of its many desirable features, the most important of which include large space-bandwidth product, immunity to electromagnetic interference (EMI), and reduced crosstalk [2]. Great research efforts have been involved in the implementation of optical interconnect at the board-to-board level [3,4].

Bus architecture has many advantages compared with point-to-point interconnects. Previously reported optical bus architectures, however, suffer from large variation among the optical signal fan-outs [3,4]. The larger the variation is, the more difficult the integration of optical detection elements will become. Based on substrate-guided-wave optics, we proposed a new architecture concept called the centralized optical backplane (COB) [5], as shown in Fig. 1. COB keeps the advantages of bus architecture while at the same time providing uniform optical signal fan-outs. In this paper, the first version of an experimental prototype of the COB architecture was demonstrated to verify its feasibility.

2. Implementation of COB using holographic gratings

Single and multiplexed volume holographic gratings have been used for board-to-board level optical interconnect [3,4]. The photopolymer-based volume hologram is an attractive option for making high-efficiency gratings. Equal-strength double-grating holograms were recorded in DuPont HRF-600X014 photopolymer films as specified by the COB architecture [5]. The film's thickness is 20 μm. The 532 nm line of 0.2 W from a Verdi laser was used for making all exposures. The film has little response at 850 nm, which allows in situ monitoring at this wavelength. As shown in Fig. 2, the diffracted light from an 850 nm probe laser was monitored to measure the dynamic diffraction efficiency.

The dynamic properties of single-grating formation in dry photopolymer films were examined first. A series of single-grating holograms was recorded for which the exposing illumination was stopped before the maximum saturation in the diffraction efficiency was reached. Fig. 3 shows the diffraction efficiency as a function of post-threshold exposure time during and after the exposure. After the

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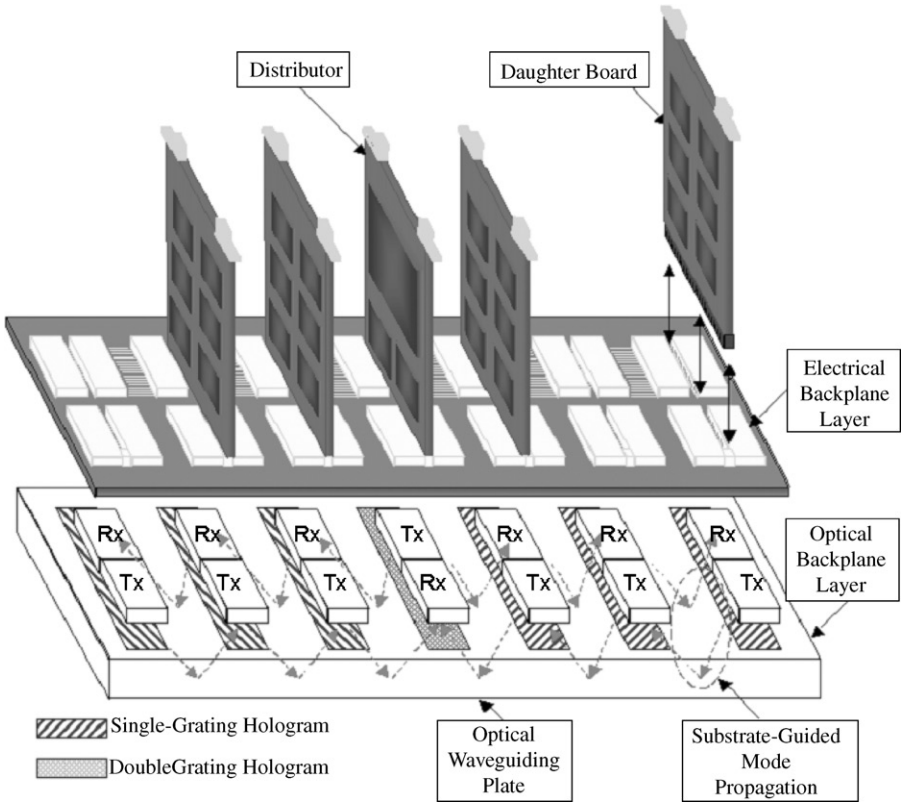

Fig. 1. Schematic illustration of the COB architecture.

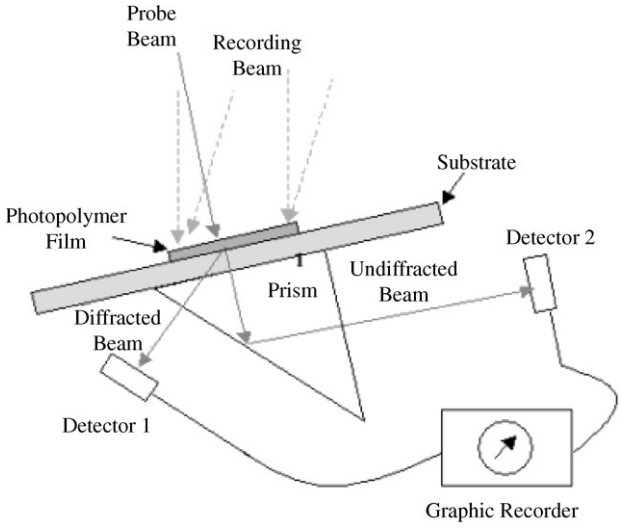

Fig. 2. Setup for the hologram recording with in situ monitoring.

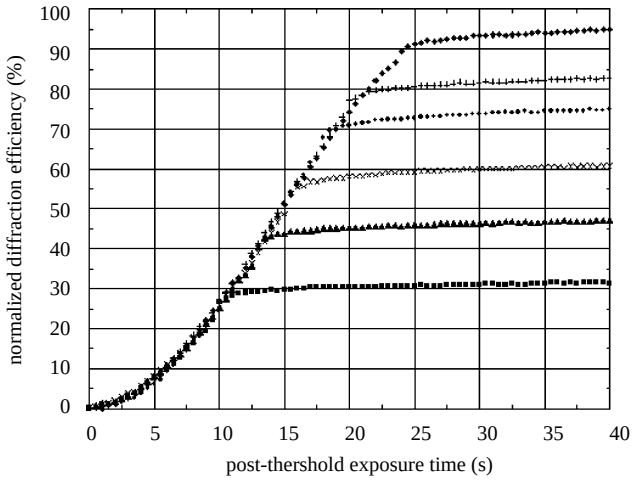

Fig. 3. Diffraction efficiency versus post-threshold exposure time, where η_{stop} is (■) 26%, (▲) 37%, (×) 48%, (●) 62%, (+) 73%, and (♦) 87%, respectively.

termination of the exposure, the diffraction efficiency continues to increase until a saturation value is reached. This increment depends on the diffraction efficiency η_{stop} at which the exposing illumination is stopped. The data in Fig. 3 show that the value of diffraction efficiency increased by, respectively, 5%, 10%, 13%, 13%, 10%, and 8% after the exposing illumination was stopped at 26%, 37%, 48%, 62%, 73%, and 87%. To make a single-grating hologram with the desired diffraction efficiency, η_{stop} is a key parameter to control. Fig. 3 can be used as a guide to find the corresponding η_{stop} for the desired diffraction efficiency.

To examine the dynamic properties of double grating formation in dry photopolymer films, a series of double-grating holograms was recorded. One more detector was used to

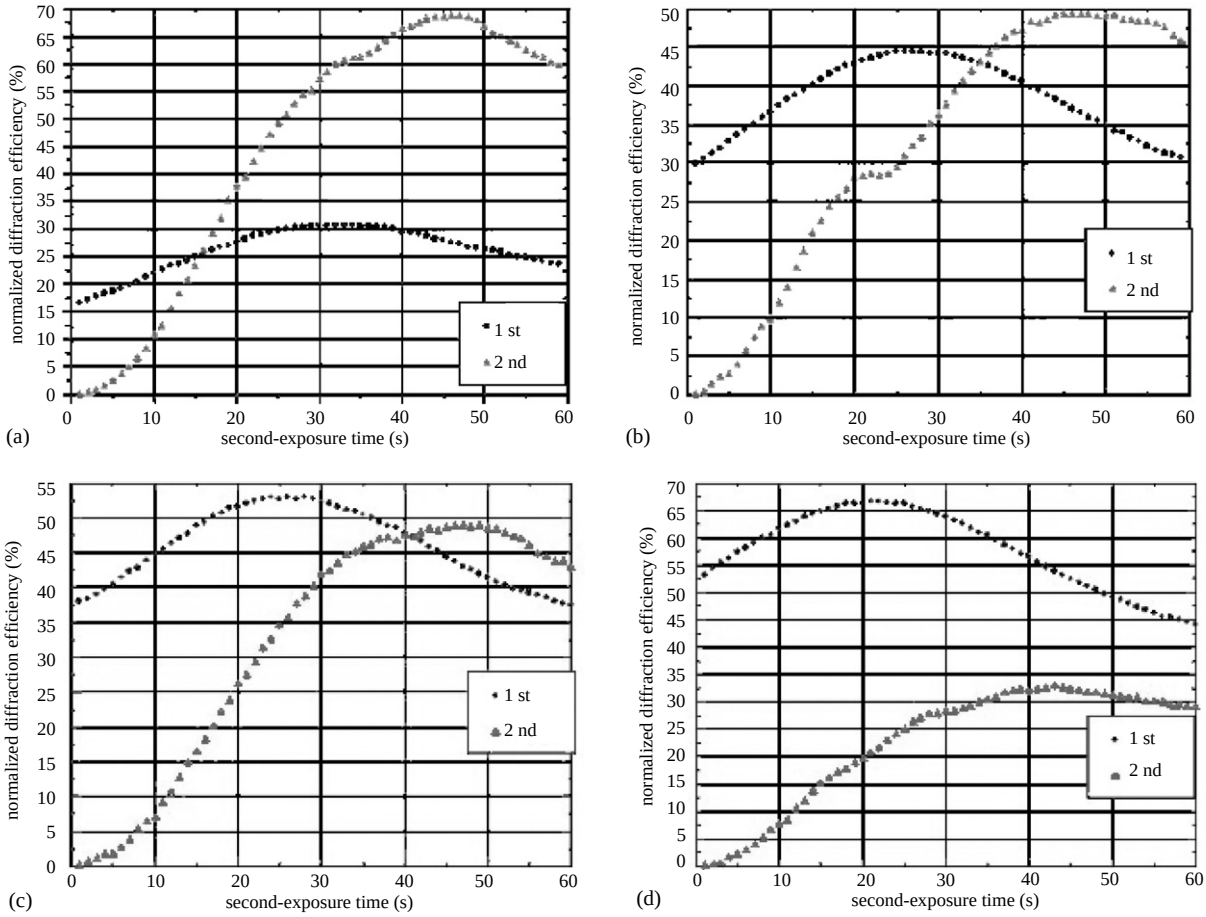

Fig. 4. Diffraction efficiency versus second-exposure time, where $\eta_1(0)$ is (a) 16%, (b) 30%, (c) 37%, and (d) 52%, respectively.

monitor the probe beam diffracted by the second grating during the second exposure. The experiments were conducted as follows: (1) the first exposure was stopped when the first grating's diffraction efficiency, η_{stop}, reaches a specific value; (2) the substrate was rotated 180°; (3) the film was exposed to the recording beams again to form the second grating. To ensure the stability of the first grating and the repeatability of the experiments, some waiting time is required such that the second step takes 30 s. Fig. 4 shows the diffraction efficiency of the two gratings as a function of second-exposure time. During the second exposure, the diffraction efficiency of the first grating increases to a saturation value, and then rolls down with further exposure. The second grating shows the same behavior but lags behind that of the first grating. Our objective is to characterize the crossing point where the two gratings have the same diffraction efficiency η_{equal}, which depends on the first grating's diffraction efficiency $\eta_1(0)$ at which the second exposure is started. As discussed previously the dynamic properties of single-grating formation, $\eta_1(0)$, which is also the saturation diffraction efficiency after the termination of the first exposure, are determined by η_{stop}. The data in Fig. 4(a)–(c) show that η_{equal} was, respectively, 26%, 43%, and 47% in the case that $\eta_1(0)$ was 16%, 30%, and 37%. On the other hand, the data in Fig. 4(d) show that η_{equal} did not exist in the case that $\eta_1(0)$ was 52%. To make a high-efficiency equal-strength double-grating hologram, $\eta_1(0)$ is a key parameter to control. Fig. 4 can be used as a guide to find the optimal $\eta_1(0)$, and then Fig. 3 can be used to find η_{stop} for the corresponding $\eta_1(0)$.

Following the procedure described above, we obtained high-efficiency equal-strength double-grating holograms for the demonstration of uniform optical signal fan-outs as shown in the inset of Fig. 5. As specified by the COB architecture [5], an equal-strength (47%/47%) double-grating hologram was integrated at the center of the optical waveguiding plate. The diffraction angles of the holographic gratings were 45°. Each end of the plate had a 22.5° bevel coated with aluminum to provide a nearly 100% reflection efficiency. The fan-out variation was measured to be within 2.5%.

3. Microprocessor-to-memory interconnect system

The prototype including a microprocessor (MC68HC812A4, Motorola Inc.) and two external memory boards is shown in Fig. 5. Although the system clock is 16 MHz, which is limited by the capacity of

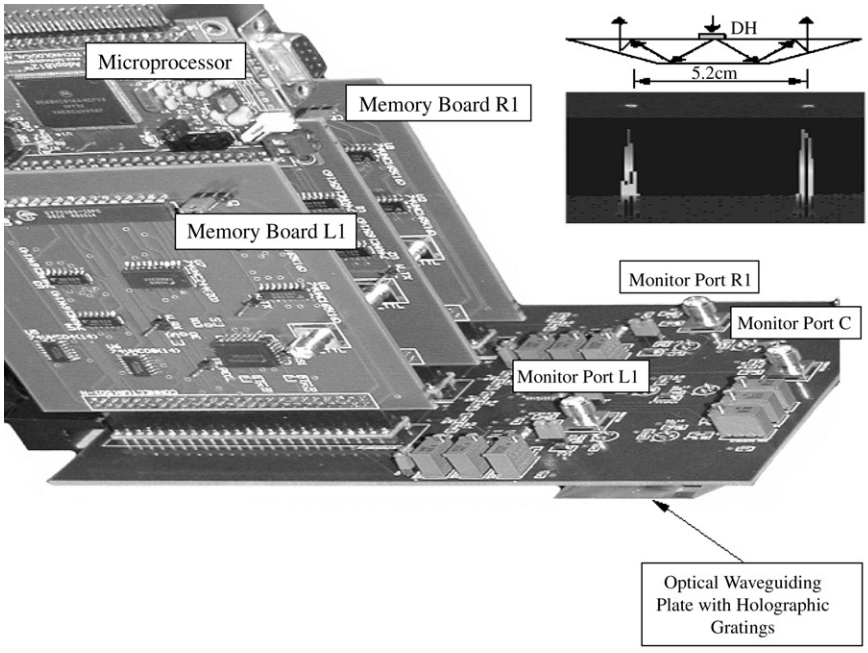

Fig. 5. The three-board microprocessor-to-memory interconnect system, where the monitor ports indicate the modulation current of their corresponding VCSELs. The inset shows the uniform fan-outs.

MC68HC812A4, it is sufficient for our proof-of-concept purpose. The required connectivity for the microprocessor-to-memory interconnect was achieved by using a COB. The microprocessor board was inserted into the center slot, and two memory boards, L1 and R1, were inserted into their corresponding slots. For data transactions, shift registers were used to serialize data at the transmitter side and de-serialize data at the receiver side. According to the addresses specified in the instructions, the microprocessor can exchange data with the memory on the selected memory board through the COB.

Optoelectronic interface modules, consisting of transmitters and receivers, implement electrical-to-optical and optical-to-electrical conversions. A transmitter module consists of an 850 nm VCSEL and a laser driver that accepts differential PECL inputs and provides complementary output currents. A receiver module consists of a photodetector/transimpedance amplifier and a post-amplifier that accepts a wide range of voltages (10–1200 mV) while providing a constant-level output voltage (PECL).

4. Experimental results

The PCB design was optimized to support high-speed processing elements at data rates up to 1.25 Gbps. Eye patterns were measured to characterize the performance of the optoelectronic interface modules. The pseudo-random bit sequence (PRBS) from a pulse generator (HP8183A) was used as the input of a laser driver in an optoelectronic interface module. The output optical signal was transferred through the optical waveguiding plate with volume holographic gratings and was then detected by a receiver in another optoelectronic interface module. Along with the trigger signal from the pulse generator, the output signal from the receiver was fed into a digital communication analyzer (HP83480A) to measure eye patterns. Fig. 6 shows the eye pattern at a data rate of 1.25 Gpbs. This result justifies that these optoelectronic interface modules are capable of supporting high-speed processing elements at such a data rate.

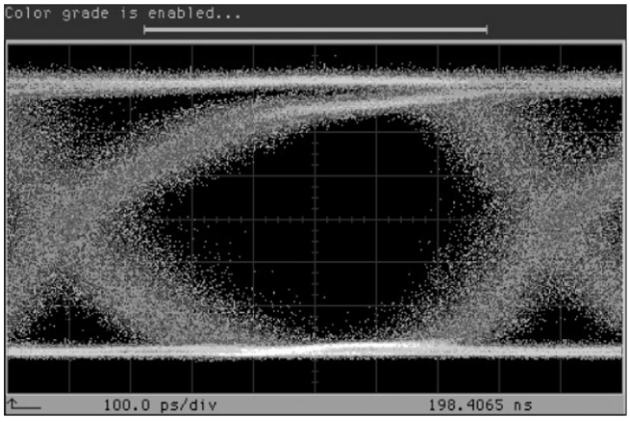

Fig. 6. Eye pattern of the optoelectronic interface modules at a data rate of 1.25 Gbps.

To visualize the test of the required connectivity for the microprocessor-to-memory interconnect, we ran the prototype under an infinite loop operation. This loop operation contained a data transaction function in which the microprocessor wrote an 8-bit data to the memory on the selected

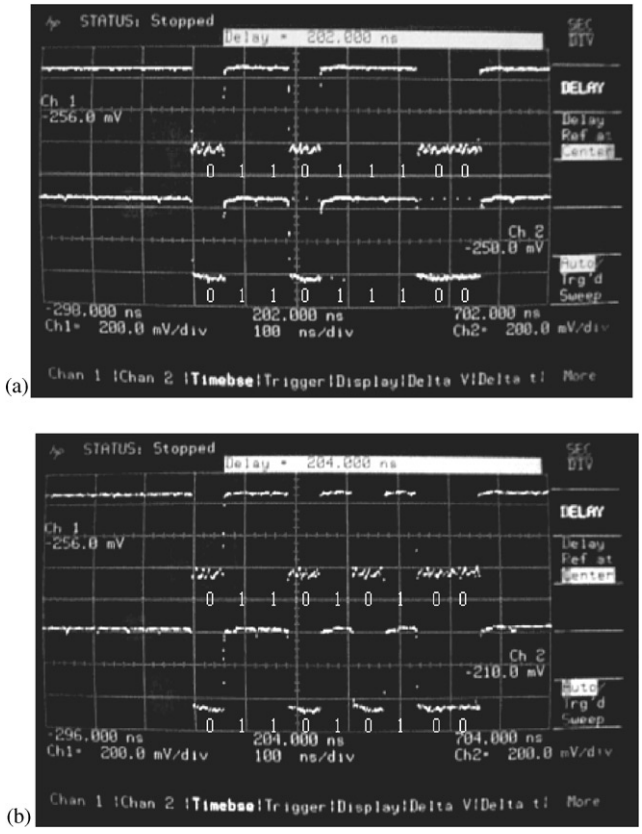

Fig. 7. Modulation current of the VCSELs in the optoelectronic interface modules.

memory board, and then read it back from that memory. As shown in Fig. 5, we designed several test ports from which we could check the data flow. Monitor port C indicated the level-inverted modulation current of the VCSEL on the microprocessor side, and monitor ports L1 and R1 indicated the level-inverted modulation current of the VCSELs on their corresponding memory sides. In Fig. 7(a), Channels 1 and 2 show the waveforms of the data '0 × C4' observed at monitor ports C and L1, respectively. Along with the starting logic high bit, which is used as the synchronization bit, the serial pattern of the data '0 × C4' should be '011011100', where the last eight bits '11011100' are the data bits, in the level-inverted representation [6]. Similarly, in Fig. 7(b), Channels 1 and 2 show the expected serial pattern '011010100' of the data '0×D4' observed at monitor ports C and R1, respectively. These results prove explicitly that the data transfer correctly back and forth through the COB.

5. Conclusion

As a preliminary proof-of-concept demonstration, we designed and implemented the first version of an experimental prototype of the COB architecture in a three-board microprocessor-to-memory interconnect system. A COB was implemented using holographic gratings, and the required connectivity for the microprocessor-to-memory interconnect was achieved by using this COB. COB retains the advantages of bus architectures while at the same time providing uniform optical signal fan-outs. Furthermore, the COB architecture is of general applicability and can be applied in scenarios other than the microprocessor-to-memory interconnect demonstrated herein.

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