Optoelectronic Packaging for 16-Channel Optical Backplane Bus with VHOEs

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Abstract

A novel 16-channel optical backplane bus with volume holographic optical elements (VHOEs), operating as diffraction grating beam alignment guides, was designed and fabricated for a high-performance computing system multi-slot bus. These thin film VHOEs were fabricated to diffract light beams for each bus slot into a glass wave-guiding plate (refractive index 1.52) for total internal reflection to other slot positions. Slot-to-slot optical alignment issues, including channel crosstalk and beam alignment tolerances, were computer modeled to optimize a low cost and simple optical packaging structure. For each slot position, a 4 X 8 element optical packaging plate was then fabricated to allow insertion of 16 VCSELs and 16 Photodiodes, each in an individual TO-46 can.

Through the VHOE, the slot-to-slot fan-out received beam intensities were experimentally measured for each of the 16 channels and found to be in the range of 90 μW ~ 150 μW. This 90 μW minimum fan-out power is 5dB greater than the receiver sensitivity requirement. In this study, the maximum 10 Gbps single channel bandwidth was tested and a 1.6 Gbps aggregate bandwidth was also demonstrated through a three slot 16-channel optical backplane bus. This aggregate bandwidth was limited by an electronic element in the receiver circuit (155 Mbps PD-TIA) and processor (100 Mbps FPGA). With the system's measured optical isolation of greater than 80dB, and suitably fast receiver electronics, simulation modeling indicates that Terabit per second bus data rates can be achieved in inexpensive, mechanically robust and reliable form factors.

Index Term – Optical Backplane Bus, Volume Holographic Optical Elements (VHOEs), VCSEL, Photodiode, Lateral and Angular Misalignment, Optical Packaging Plate.

1.Introduction

Due to the rapid and wide expansion of the internet service, every personal computer is now connected to every other computer all over the world. The number of computers and servers connected with the internet has increased every year. The amount of data also increased because large amounts of data can be handled by the increased execution speed of the central process unit (CPU). The most recent International Technology Roadmap for Semiconductors (ITRS) projects that while per-chip performance will continue to improve at a rate of approximately four times every three to four years, the number of signal pins per module will only double over the same period, and the maximum bit rate per signal pin will increase by only 35% [1]. By 2010, the requirement for off-chip

clock frequency will reach more than 12 GHz. Also, modern multiprocessor computer architectures place stringent demands on the inter processor connection schemes. Thus, the total off-chip I/O bandwidth, pin count times bit rate per pin, will increase by roughly 2.7 times, while the internal chip performance improves by four times [2] per process cycle.

An unfortunate consequence of this improvement rate mismatch is that system computing performance is not proportional to the increase in number of processors. In a typical system, processors and memory are distributed across several different nodes, and data must be constantly transferred between them as computing operations occur. The performance of multiprocessing systems is mainly limited by the bandwidth, the power consumption and delay of electrical interconnections. Electrical interconnects cannot achieve sufficiently high data rates using traditional bus architecture, so utilizing large numbers of point-to-point interconnects has become a popular choice for high speed system. Therefore, wiring congestion is a concern for high performance computing. A 10Gbps high-speed electrical backplane using point-to-point link has been demonstrated by Sinsky *et al.* [3]. A bit error rate (BER) of less than 10^{-13} was achieved over an 87 cm transmission line using duobinary signal encoding. Recently, data transmission at 25 Gbps over a 61 cm link (15.25 Gbps·m) on an electrical backplane was demonstrated by the same group [4]. Electrical backplane can support, in theory, 100 Gbps Ethernet applications using conventional backplane design techniques (four channels at 25 Gbps). However, a detrimental drawback of the approach is the high signal loss over the link of −50 dB at 25 GHz due to skin effects and dielectric losses in the FR4 material [5].

On the other hand, optical backplanes permits different daughter boards to share the transmission channel while maintaining extremely high data rate, and therefore does not have wiring congestion problem. We demonstrated the first optical backplane bus with the volume holographic gratings at 15 Gbps data rate per channel [6,7]. In such an optical backplane, a bus architecture is retained to fulfill the task of broadcasting and transmission channel sharing, while the potential data rate is comparative to or even higher than that in electrical point-to-point type backplane, as long as high-speed electro-optical transceivers are available. The optical backplane bus uses optical signal to realize communications for board-to-board interconnection. Each board is equipped with optoelectronic transceivers (VCSELs and photodiodes) for the emission and detection of modulated optical signals. Several optical bus architectures based on the optical backplane have been proposed including the substrate-mode guided-wave bus system implemented with wave-guiding plates and holographic grating elements [7,8,9,10] and the free-space bus systems implemented through free-space optical interconnections [11,12].

In this paper, a novel 16-channel optical backplane bus with VHOEs was fabricated and successfully demonstrated with a computing system involving processor and memory modules. As shown in Fig. 1, the optical backplane bus contains TO-46-CAN packaged 1.5 Gbps VCSELs and 622Mbps photodiodes (with 155 Mbps TIA) as an optical transmitter and receiver, respectively. The volume holographic grating films are recorded to diffract light beams (λ = 850 nm) into a glass wave-guiding plate (refractive index 1.52) for total internal refraction. To reduce packaging difficulties, a novel 4 X 8 optical packaging plate is designed for 16-channel optical backplane bus system. Packaging issues including crosstalk and alignment tolerance were theoretically studied to design optical packaging structure. Although each individual channel shows the maximum bandwidth of 10 Gbps,

the system demonstration reported herein is limited by the processor (Xilinx FPGA, Virtex4-FX60) which has 100 Mbps channel data rate.

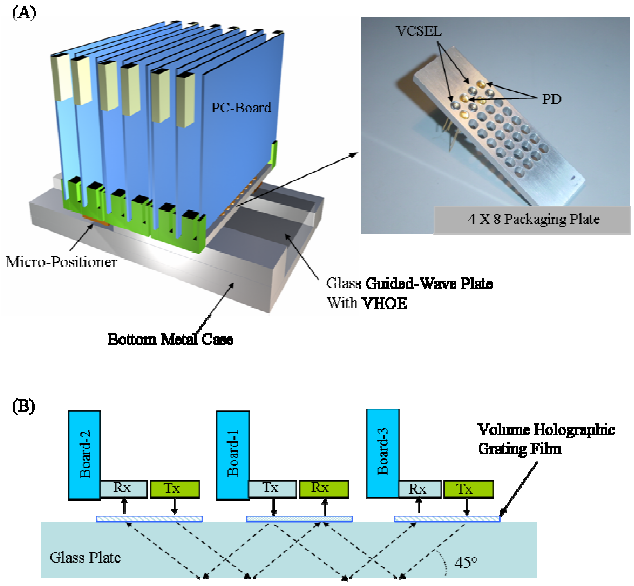


Figure 1 (A) Schematic 3-D view of 16-channel optical backplane bus with the volume holographic gratings. A 4 X 8 optical packaging plate for packaging of optoelectronic devices (16 VCSELs and 16 Photodiodes are packaged alternatively). (B) Schematic view of optical signal redirection mechanism by the volume holographic gratings and a glass guided-wave plate. (▩ : double grating hologram, ▨ **:** single grating hologram)

II. Fabrication of Volume Holographic Grating Films and Optical Packaging Plates

The photopolymer-based volume hologram is an attractive option for making high-efficiency gratings. A single hologram grating is recorded in DuPont photopolymer (HRF-600) film to precisely redirect input/output signal beams at 45^{o} zigzag bouncing angle. The thickness of the photopolymer film is 10 μm. The Verdi laser (λ = 532 nm) is used for recording photopolymers. The photopolymer emulsion is insensitive at 850 nm, which allows *in-situ* monitoring at this wavelength. The diffracted light from an 850 nm probe laser was monitored to measure the dynamic diffraction efficiency.

There are 4 pieces of the volume holographic films on the glass substrate. *In-situ* monitored hologram efficiencies, during the recording process [13], are 54.9%, 45.4%, 68.4% and 42.5%, respectively. The size of the hologram film on the center and the sides (A and B) are 50 X 30 mm^2 and 50 X 40 mm^2, respectively. To reduce the output beam diverge angle of VCSEL and to converge the input beam of photodiode, an individual dome-lens installed TO-46-CAN packaged VCSEL and photodiodes are used in this study.

Due to the optical crosstalk between the adjacent optical bus lines, the minimum pitch between two adjacent photodiodes must be determined according to the requirement of the optical signal-to-noise (SNR) ratio. Since commercial TO-46-CAN packaged VCSEL and photodiode have the same physical radius, the minimum pitch in 4 X 8 row-

and-column pattern packaging is 4.77 mm.

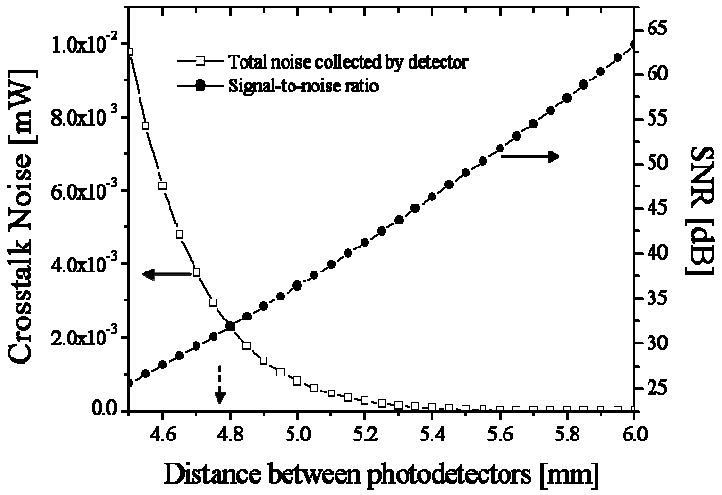


Figure 2 Calculated crosstalk and optical signal-to-noise ratio (SNR) as a function of photodiode pitch (with R = 2.38 mm) in the row-and-column pattern packaging plate.

Fig. 2 shows that the calculated signal-to-noise ratio and crosstalk noise as a function of the distance between photo-detectors [PD 622Mbps & TIA 155Mbps]. As the pitch increases above 5 mm, crosstalk noise decreases and then disappeared below 1 μW. Also the geometrical optical path-length (30 mm) through VHOE and mechanical machining tolerances (± 0.25 μm) are considered in designing 4 X 8 row-and-column pattern packaging plates. In this study, 5.5 mm pitch optical packaging plates are fabricated. The distance between photodiodes after packaging, the diagonal distance in the row-and-column pattern, is 7.78 mm. Therefore, as based on Fig. 4, the optical crosstalk noise effect, measured at greater than 80 dB cross signal rejection, can be disregarded between two detectors in this packaging plate.

The influence of angular misalignment on lateral misalignment arises from the phase mismatch between the input signal beam and the grating vector when the incident angle deviates from the Bragg angle. Fig. 3-(A) shows the phase matching conditions of a volume holographic grating for surface-normal coupling.

For the Bragg condition, the relation between the incident angle and the diffracted angle is

$$\begin{pmatrix} -\sin\gamma \\ \cos\gamma \end{pmatrix} = \begin{pmatrix} \dfrac{\sin\theta}{n} - \dfrac{K}{\beta}\sin\phi \\ \left(1 - \dfrac{\sin^2\theta}{n^2} - \dfrac{K}{\beta}\cos\phi\right)^{1/2} \end{pmatrix} \qquad (1)$$

where n is the refractive index of the hologram, $\beta(=2\pi n/\lambda)$ is the propagation constant of light with wavelength λ, and the meaning of γ, θ and K are as shown in Fig. 3-(A). After eliminating ϕ and differentiating the resulting equation, we have

$$\Delta\gamma = \frac{\left[\sin\theta - n\left(\frac{K^2}{2\beta^2} - 1\right)\sin\gamma\right]\cos\theta}{\left[\left(\frac{K^2}{2\beta^2} - 1\right)\sin\theta - n\sin\gamma\right]n\cos\gamma}\Delta\theta \qquad (2)$$

A variation of the angle of the input light beam leads to a spatial shift of the fan-out beam on the device surface of

$$\Delta L = \frac{\tan(\gamma + \Delta\gamma) - \tan\gamma}{\tan\gamma} \cdot L \qquad (3)$$

where, L is the distance between input and output beam positions.

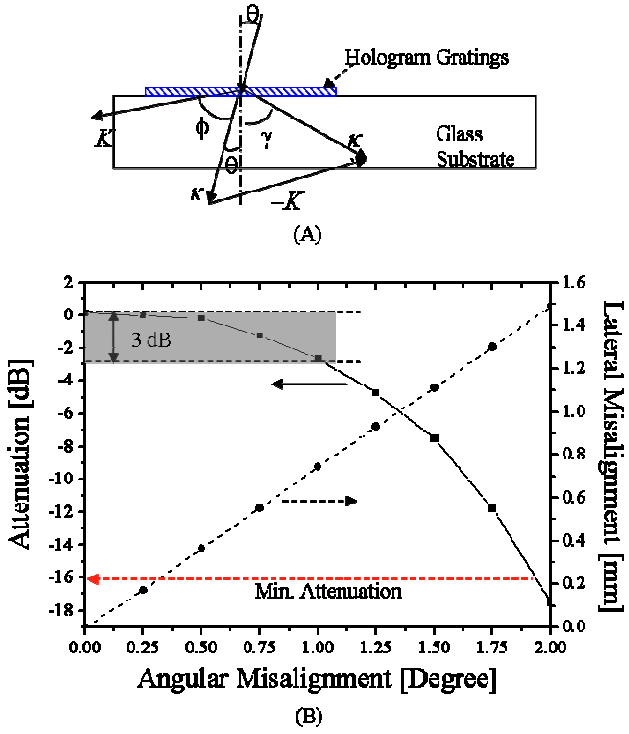


Figure 3 (A) Phase-matching diagram correlating the grating vector K, the incident beam k, and the diffracted beam k` for a slanted holographic grating element. (B) Measured fan-out power loss and calculated lateral misalignment (ΔL) as a function of input beam angular misalignment ($\Delta\theta$)

Fig. 3-(B) shows the calculated lateral deviation (ΔL) as a function of the incident angle ($\Delta\theta$) and measured fan-out power intensity variations as a function of in-put beam angular misalignment ($\Delta\theta$). Experimental results show that a 1^o angular misalignment accompanied by 3dB fan-out power loss and it is related to a 0.76 mm lateral misalignment,

concurrently. To obtain maximum fan-out power through VHOE, during VCSEL packaging, the angular misalignment is minimized below 1^{o} and induced lateral misalignment can be adjusted using a micro-stage assembled with an optical packaging plate as shown in Fig. 1.

III. VCSEL Packaging to Equalize Fan-out Beam Broadcasting

To optically interconnect 4 X 8 Tx-Rx arrays using VHOEs as shown in Fig. 4, the recorded volume holographic grating films are attached on the glass substrate. The optical input signal beams, vertical to the holographic film surface, are refracted at 45^{o} by slanted fringe structures of transmission volume holographic gratings. Due to the total internal reflection, coupled input beams are propagating through a glass wave-guiding plate and then coupled out by the matched holographic grating films.

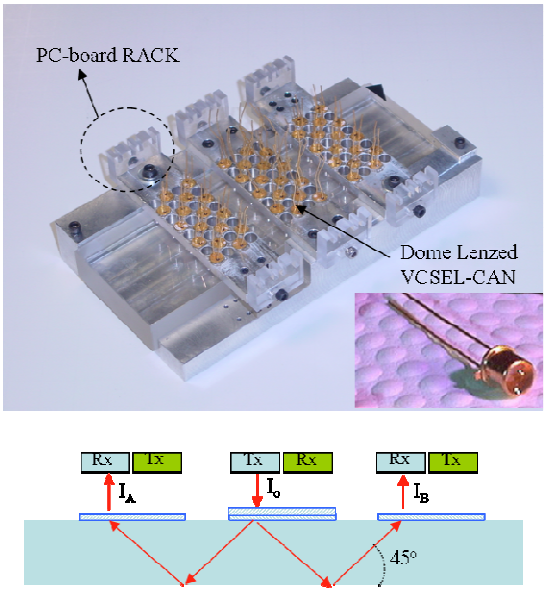


Figure 4 Assembled optical packaging components. 48-VCSELs are assembled onto 4 X 8 optical packaging plates. A glass substrate with the volume holographic gratings is assembled by a bottom metal case structure. Electrical PC-boards are assembled using rack structures. (The bottom figure shows a schematic view of equalized fan-out beam directions through the volume holographic gratings)

Fan-out beam intensity depends upon not only the diffraction efficiency of the hologram film but also the input beam incident angle as shown in Fig. 5. Therefore, the uniformity of the fan-out beam intensity through VHOEs is one of the critical issues in this system. The measured surface area of a single hologram film, covering 4 X 8 packaging array, is 21.28 X 43.3 mm^2. A 2 mW (1.88 V / 11 mA) VCSEL beam is used as an input source (I_o). 32-point fan-out beam intensities (I_A and I_B) are measured using 4 X 8 packaging plates (4-columns and 8-rows) shown in Fig. 4. Experimentally measured 3-D fan-out beam intensity profiles are shown in Fig. 5. From the system power budget point of

view, the fan-out beam intensities should be larger than the minimum value of photo-sensitivity, 20 μW, of photodiode with TIA to provide decent power margin. All fan-out beam intensity values through VHOEs are in the range of 53.2 μW ~ 165.6 μW. The average intensity values in the center and the edge of holographic grating film are 135 μW and 80 μW, respectively.

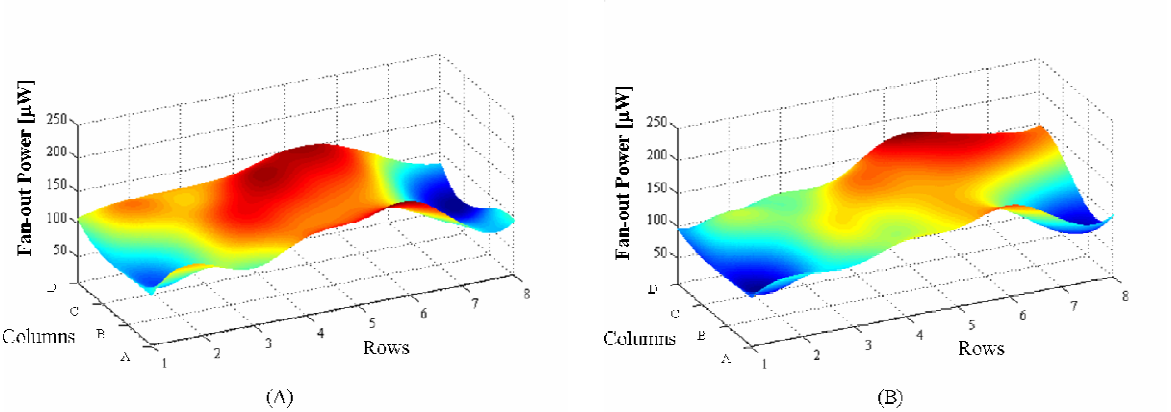


Figure 5 Measured equalized fan-out power (I_A & I_B shown in Fig.5) uniformity through volume holographic grating films.(A) Equalized fan-out power distribution through $I_o \rightarrow I_A$, (B) Equalized fan-out power distribution through $I_o \rightarrow I_B$

Since 16-VCSELs and 16-photodiodes are alternatively packaged into 32 packaging holes (4 X 8 row-and-column pattern as shown in Fig. 1), 16-channel fan-out powers from the center plate to the sides (left and right), and vise versa, are measured. During VCSEL packaging, fan-out beam intensities are simultaneously monitored and the optimum packaging position is adjusted to achieve even fan-out power through VHOEs.

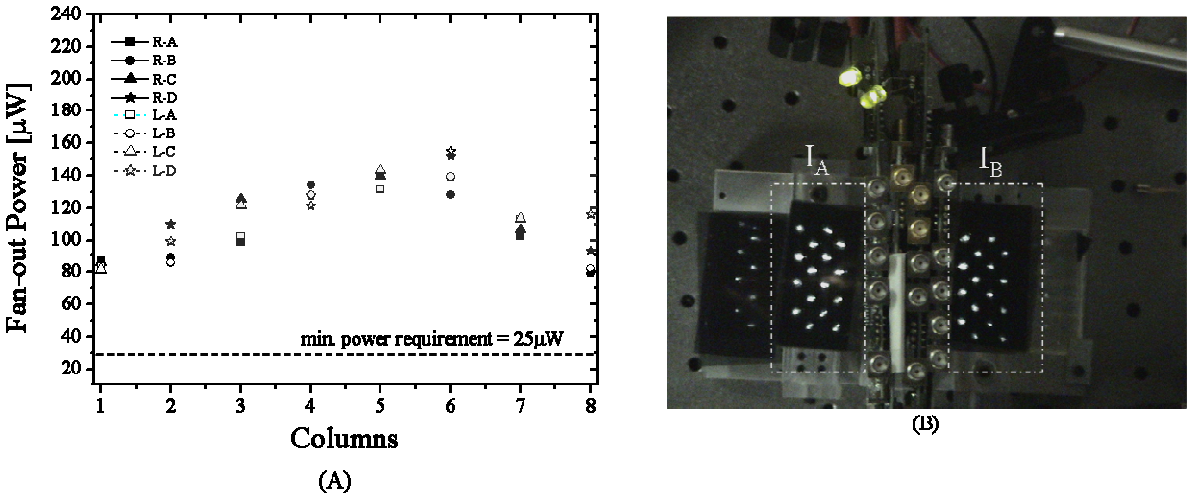


Figure 6 (A) Measured 16-channels equalized fan-out powers (I_A & I_B shown in Fig.5) through VHOEs [plate(R/L)-row, I_0 = 2 mW] (B) Far-field images of 16-channel equalized fan-out beams through VHOEs [16 beam spots inside the boxes (I_A & I_B shown in Fig.5) show the far-field images of 16 VCSEL beams diffracted by volume holographic optical elements (VHOEs)]

Fig. 6-(A) shows that 90% of 16-channel fan-out beam intensities are in the range of 90 μW ~ 150 μW. Moreover, the measured minimum fan-out power is 78.9 μW which is 5dB higher than the minimum power requirement of this system. The far-field image of 16-channel equalized fan-out beam is measured by a CCD camera as shown in Fig. 6-(B). Broadcasting 16-channel beam spots are clearly shown on the both sides of the package plate.

IV. System Assembly and Performance Test

All optical components, VCSELs, Photodiodes and VHOEs, are precisely assembled using optical packaging plates and the metal case structure shown in Fig. 4. The center packaging plate is physically bolted on the case. Two side packaging plates are designed to move laterally within a range of ±1.5 mm using micro-stage. In each optical plate, 16-VCSELs and 16-Photodiodes are arranged in row-and-column pattern as shown in Fig. 1.

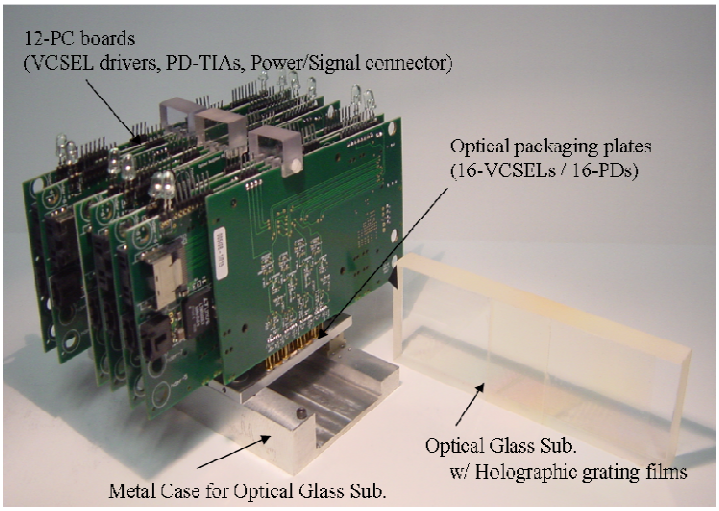


Figure 7 Assembled 16-channel optical backplane bus. PC-boards containing VCSEL drivers (3.2Gbps), PD-TIAs (155 Mbps), power/signal connector are connected with optoelectronic devices. An optical glass substrate with the volume holographic grating films

Optical guided-wave glass plate with the volume holographic grating films is also inserted into the case and then mechanically assembled. A total of 48-VCSELs and 48-PDs are precisely aligned and then packaged to get maximum fan-out power distributions. Electrical control boards are located on the top of the packaging plate as shown in Fig. 7.

Each electrical board contains 4-VCSEL drivers and 4-PD-TIAs (trans-impedance amplifiers). Four PC-boards are assembled on a single optical packaging plate to control the 16-VCSELs and 16-photodiodes. A total of 12 PC-boards are plugged to control 48-VCSELs and 48-photodetectors in this system.

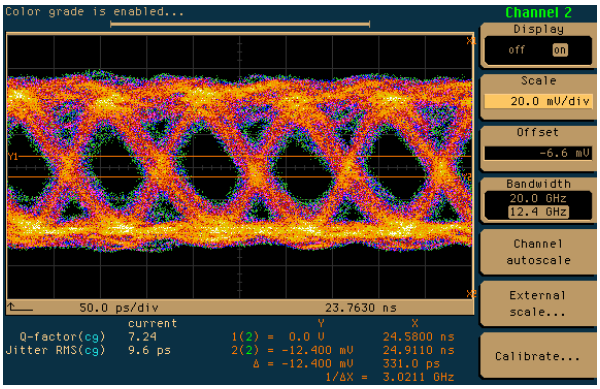
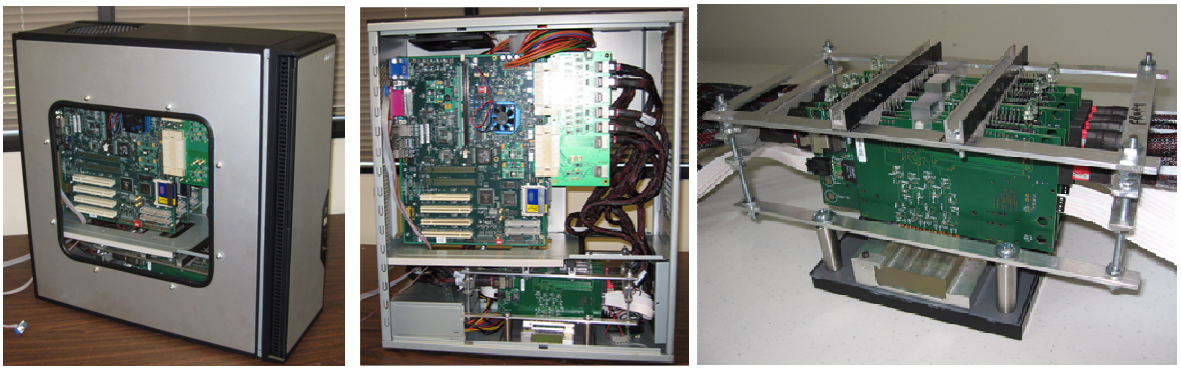


Figure 8 10 Gbps single channel eye-diagram through optical backplane bus system using Thin Film Hologram Grating.

Fig. 8 shows a single channel eye-diagram at 10 Gbps through the optical backplane measured by a digital communication analyzer (HP-83480A). The pulse pattern generator provides the modulation by generating a 2^{23}-1 pseudorandom bit sequence (PRBS) non return-to-zero (NRZ) pattern. Measured Jitter-RMS and Q-factor are 9.6ps and 7.24, respectively. Although each individual channel has the maximum bandwidth of 10 Gbps, the system demonstration reported herein is limited by the processor (Xilinx FPGA, Virtex4-FX60) which has 100 Mbps channel data rate.

All channels are individually tested and optical connection performance between VCSEL and photodiode through VHOEs is verified. All optical and electrical components are connected properly using cable connectors. The optical part (shown in Fig 7) consists of the hologram based optical backplane and 12-PC-boards containing VCSEL drivers, PD-TIAs, power connectors and signal connecters.



(A) (B) (C)

Figure 9 (A) Demonstration setup for high performance computing system with 16-channel optical backplane bus. (B) Inside view of computing system, FPGA (Xilinx Virtex-4) and memories control electrical signals through 16-channel optical backplane bus which transfer data optically. (C) Packaging set-up for Optical backplane bus.

The electrical part consists of 3 signal control boards and computing modules to operate a high speed computing system. The high speed computing system demonstration is performed using the setup shown in Fig. 9. In this demonstration, the computing system controls two FPGA boards to monitor BER (Bit Error Rate) test using 10,000 date packet per single channel. All 16 channels are monitored simultaneously. BER test result shows no error data transfer through the 16-channel optical backplane bus with VHOEs. Total 64 channels including 32 broadcasting channels are successfully demonstrated with the commercial computing system. With the system's measured optical isolation of greater than 80dB, and suitably fast receiver electronics and processor, simulation modeling indicates that Terabit per second bus data rates can be achieved in inexpensive, mechanically robust and reliable form factors.

V. Conclusions

A novel 16-channel three slot optical backplane bus is designed and fabricated using thin film volume holographic gratings to demonstrate a high-performance computing system multi-slot bus. Individual channel performs the maximum bandwidth of 10 Gbps. In this study, a 1.6 Gbps aggregate bandwidth was demonstrated through a three slot 16-channel optical backplane bus. In this demonstration, this single channel bandwidth limitation is due to an electronic element in the receiver circuit (155Mbps PD-TIA) and processor (100 Mbps Xilinx FPGA). All channels are individually tested and optical connection performance between VCSEL and photodiode through VHOEs is verified.

Thin film volume holographic gratings were fabricated to refract light beams into a glass wave-guiding plate for total internal reflection. Through the VHOEs (Volume Holographic Optical Elements), equalized fan-out beam intensities were experimentally measured. Packaging issues including crosstalk and alignment tolerance are theoretically studied to design a low cost and simple optical packaging structure. A 4 X 8 optical packaging plate is fabricated to assemble 16-VCSELs and 16-Photodiodes. VCSELs and photodiodes are inserted alternatively into 32-holes drilled with a 4 X 8 row-and-column pattern optical packaging plate. 16-channel fan-out beam intensities are in the range of 90 μW ~ 150 μW. Moreover, the measured minimum fan-out power is 78.9 μW which is 5dB higher than the minimum power requirement of this system.

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