Performance Analysis of 10-μm-Thick VCSEL Array in Fully Embedded Board Level Guided-Wave Optoelectronic Interconnects

Chulchae Choi, Lei Lin, Yujie Liu, and Ray T. Chen, *Senior Member, IEEE, Fellow, OSA*

***Abstract*—We introduce a simple and effective heat sink structure for thin-film vertical cavity surface emitting lasers (VCSELs) in fully embedded board level guided-wave interconnects. A 50% quantum efficiency increase is experimentally confirmed for the 10-μm thin-film VCSELs. The thermal resistance of a 1×12 embedded thin-film VCSEL array in printed circuit board (PCB) is further analyzed. The experimental results show an excellent match with the simulated results. The 10-μm-thick VCSEL had the lowest thermal resistance and the highest differential efficiency compared to 250-, 200-, 150-, and 100-μm-thick VCSELs. A substrate removed VCSEL can be used in fully embedded board level optical interconnects without special cooling techniques.**

***Index Terms*—Embedded optical interconnects, PCB, substrate removal, thermal resistance, VCSEL.**

I. Introduction

THE capability of high-speed data transfer rate is pivotal in high performance computer systems where interchip and board to board interconnects made from electrical transmission lines are the major bottlenecks. Electrical transmission line is inherently affected by crosstalk, skew, and reflection due to parasitic capacitance coupling and impedance mismatch in the bus architecture. Several optical interconnect approaches were introduced to resolve such limitations [1]–[4]. These approaches used hybrid integration where electronic and optoelectronic components were placed on the same surface of the platform using guided-wave or free-space optics. The reliability of these systems due to packaging vulnerability is a paramount concern.

We employed fully embedded PCB level optical interconnects to make the packaging reliable and robust [5]. It not only provides process compatibility with a standard PCB process but also reduces the footprint of the PCB by fully embedding all optical components, such as light sources, channel waveguides, waveguide couplers and detectors, among other electrical interconnection layers as indicated in Fig. 1. However, in this configuration, The VCSEL array raises thermal management concerns because it is encapsulated with thermal insulators such as polymer waveguides and bonding film (prepreg). Only the common bottom metal contact of the VCSEL array can be used as a thermal interface. The VCSEL can not operate without proper cooling. Therefore heat management of the driving VCSEL array is a critical issue in the fully embedded structure. Lee *et al.* reported the thermal management of a VCSEL based optical module [6] and Rui Pu *et al.* reported the thermal resistance of a VCSEL bonded to an IC [7]. Both papers presented valuable results but not applicable to our device structure.

This paper reports simulated and experimental results of the thermal resistance of the VCSEL, fully embedded in PCB, as a function of the VCSEL's thickness and determines the effective heat sink structure.

Manuscript received October 14, 2002; revised March 7, 2003.

The authors are with the Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX 78758 USA.

Digital Object Identifier 10.1109/JLT.2003.812162

II. Fully Embedded Board-Level Optoelectronic Interconnects

All optical components including VCSEL arrays, photodetector arrays and planarized waveguide arrays are fully embedded among electrical layers in the board level optical interconnects. As a result, it simplifies the assembly steps at the final laminating stage using standard PCB manufacturing procedure. Generally, $5 \sim 10$ mil (127 to 254 μm) thick copper laminated polymer layers and 4 mils thick (100 μm) bonding films are used in multi layer PCB. For the fully embedded structure [5], thin VCSELs and photodetectors, both 10 μm thick, are buried among electrical PCB layers. Each of the electrical PCB layers distributes electrical signals as shown in Fig. 1. Through-holes and vias are used to transport electrical signals among electrical PCB layers and also to provide electrical connections to VCSEL and detector arrays. In the fully embedded structure, the entire real estate of the top and/or bottom sides of the PCB is occupied only with microelectronic ICs which perform the designated functions including electrical to optical and optical to electrical [5].

III. Fabrication of VCSELs and Measurement of Thermal Resistance

The epitaxial structure of the VCSEL array was grown on a GaAs substrate. An etch stop layer of 100 nm thick $Al_{0.98}Ga_{0.02}$. As was grown and then a GaAs buffer layer, 40.5 pairs of n-DBR, three GaAs quantum wells, and 23 pairs of p-DBR were grown. The total thickness of the epitaxial structure is 10 μm.

The formation of the thin film VCSEL arrays started with a wet etch to make an annular shaped trench which provides isolation of each device and defines the oxide confinement region. Wet oxidation was carried out in a quartz tube furnace which

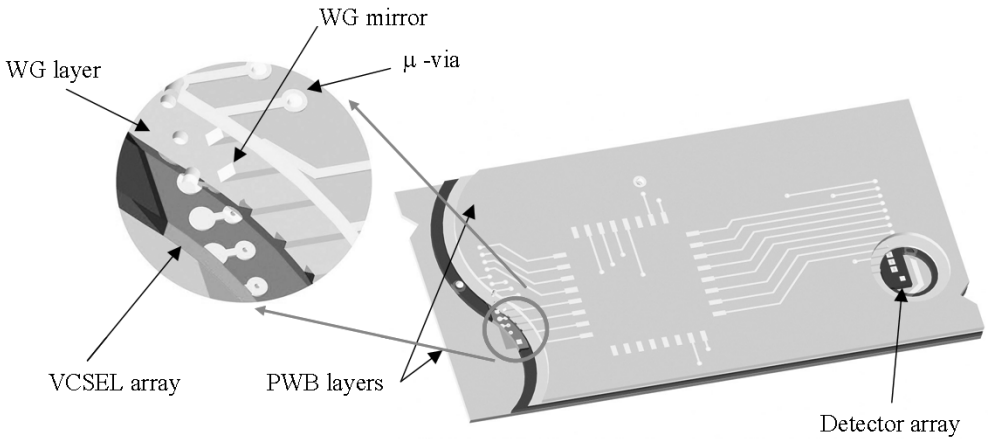
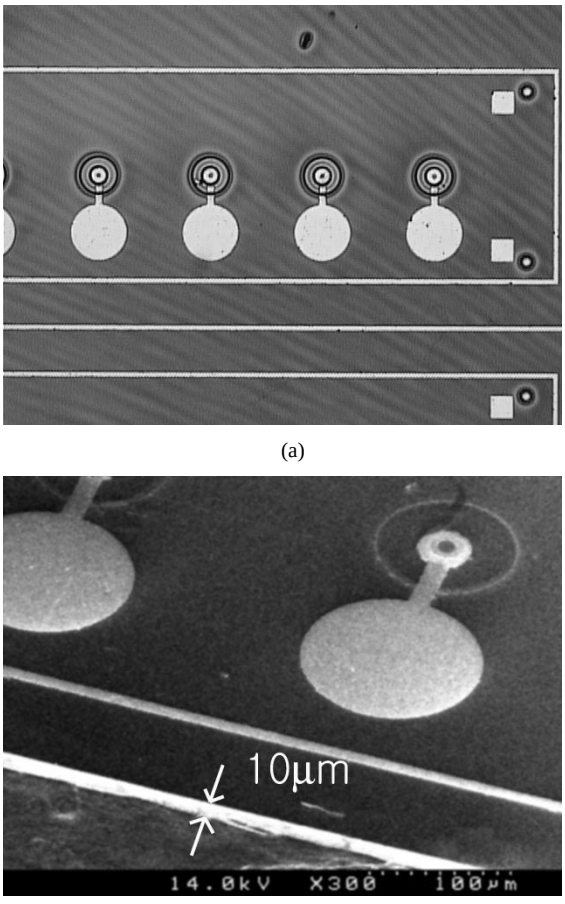


Fig. 1. Illustration of fully embedded PCB level optical interconnects. Distance between VCSEL and detector array is up to 30 cm. Thickness of the waveguide substrate is 127 μm.



(a)

(b)

Fig. 2. (a) Four parts of a VCSEL array. (b) Top: Off view of a 10-μm-thick VCSEL.

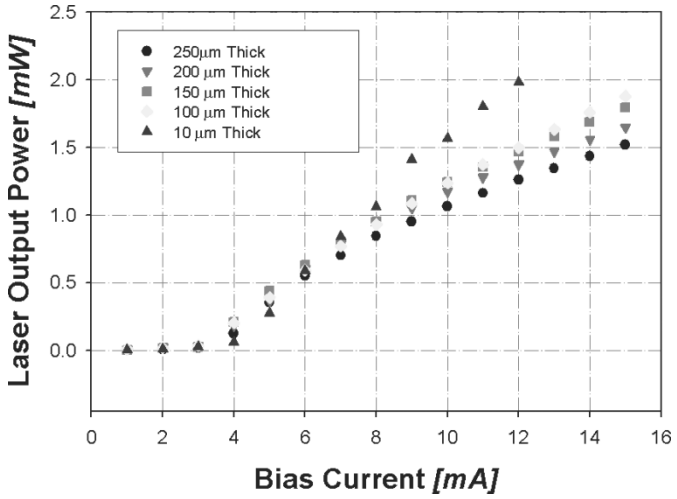


Fig. 3. *L–I* characteristics as a function of device thickness.

was held at 460 °C. Spin on glass (SOG) was coated on the entire wafer for electrical isolation and side wall sealing afterwards. The SOG opening process was followed for p-contact metallization. VCSEL array formation was followed by the substrate removal process to form the required thickness. Devices were first mechanically thinned down to 250 μm. These devices were back etched using wet etching to reduce thickness of the VCSELs down to ten micrometers [10], [11]. Fig. 2(a) shows a section of the fabricated 1 $\times$ 12 VCSEL array and Fig. 2(b) shows top-off view of a 10-μm-thick VCSEL array after substrate removal.

L–I characteristics of various thinned VCSELs are shown in Fig. 3 where the quantum efficiency of the 10-μm-thick VCSEL is increased by $\sim$50% then the driving current is above 9 mA. Reduced temperature of the active region due to higher thermal conductance increases optical gain in quantum well [12], [13]. Substrate removed VCSELs (10 μm thick) also show linear dependency even at a high injection current. The thermal resistance was calculated from the measured wavelength shift as a function of substrate temperature and dissipation power. The thermal resistance is given by $R_{th} = \Delta T/\Delta P = ((\Delta\lambda/\Delta P)/(\Delta\lambda/\Delta T))$, where ΔT is the change of junction temperature, ΔP is the change of injected power and $\Delta\lambda$ is the wavelength shift. Both $\Delta\lambda/\Delta P$ and $\Delta\lambda/\Delta T$ are experimentally confirmed.

The device under test (DUT) was laid on the top of the gallium indium eutectic metal which is used to make an electrical contact. The substrate temperature was controlled by a thermoelectric cooler (TEC).

The measured wavelength shift as a function of temperature for all devices was 0.75 Å/°C. The wavelength shifts as a function of net dissipated power were 0.59, 0.54, 0.5, 0.43, 0.36

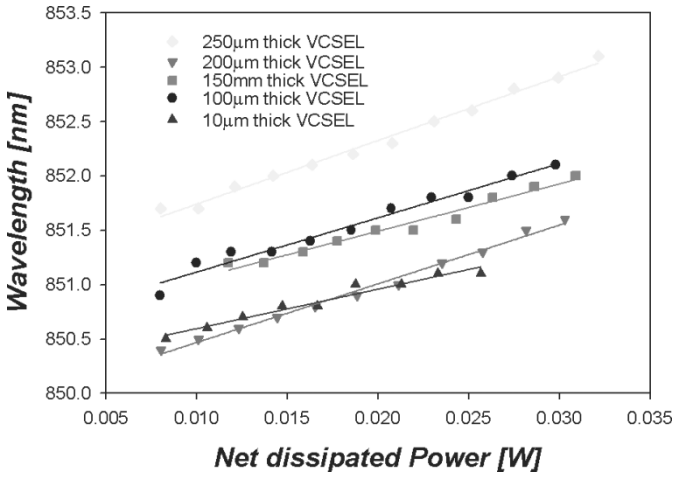


Fig. 4. Wavelength shift as a function of net dissipated power.

Å/mW, respectively, corresponding to 250-, 200-, 150-, 100-, and 10-μm-thick VCSELs as indicated in Fig. 4. The thermal resistances for 250, 200, 150, 100, and 10 μm thick VCSELs were measured to be 772, 710, 657, 572, and 478 °C/W, respectively. Note that the thickness of the 10-μm-thick VCSEL has an exclusive advantage of heat management due to the reduction of the thermal resistance shown herein.

IV. Simulation of the Thermal Resistance of an Embedded VCSEL in PCB

The VCSEL is a major heat source in a fully embedded guided-wave optical interconnect structure. The embedded VCSEL arrays are thermally isolated by surrounding insulators; therefore heat builds up and the operating temperature increases. High operating temperature may the reduce life time of the device and the laser output power. Reliable operation of the VCSEL is accomplished through proper heat management. Effective heat removal is a challenging task in the embedded structure because we have to consider packaging compatibility to the PCB manufacturing process while providing an effective and simple cooling mechanism.

In this paper, we introduce an effective heat management scheme. The n-contact metal affiliated with the bottom DBR mirror of the VCSEL die was directly electroplated with copper during the fabrication process. Thermally conductive paste was not used because it has a lower thermal conductivity than copper. Usually several tens of micrometer thick copper was deposited in copper contained acid chemical solution during PCB process. It can be used as a very good electrical and thermal passage simultaneously.

The thermal resistance of the VCSEL depends on the device structure itself and also the packaging structure. Direct bonding of a device using electroplating reduces thermal resistance of the device due to the absence of low conductivity bonding epoxy.

ANSYS software was used to perform a 2-D finite element thermal distribution analysis. The thermal conductivities of GaAs, DBR mirror and copper are 4.6×10^{-5} W/μm · K, 2.3×10^{-5} W/μm · K, and 4×10^{-4} W/μm · K, respectively [8], [9]. Heat is generated due to the Bragg reflector's resistance and imperfect conversion efficiency in active region.

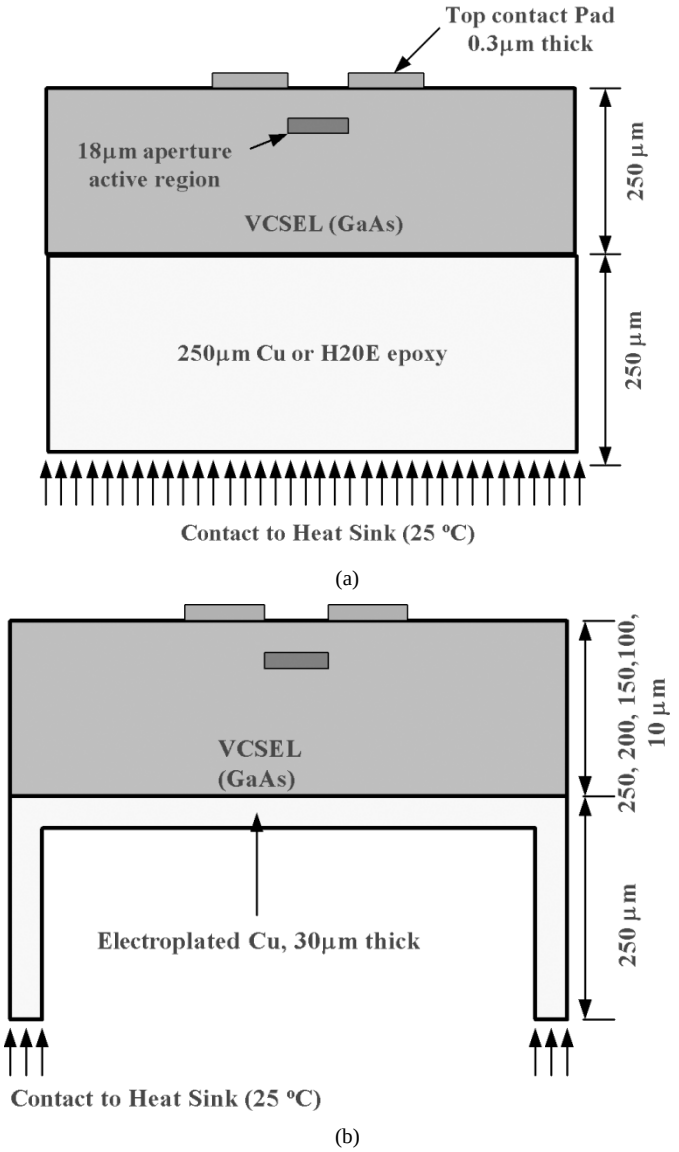
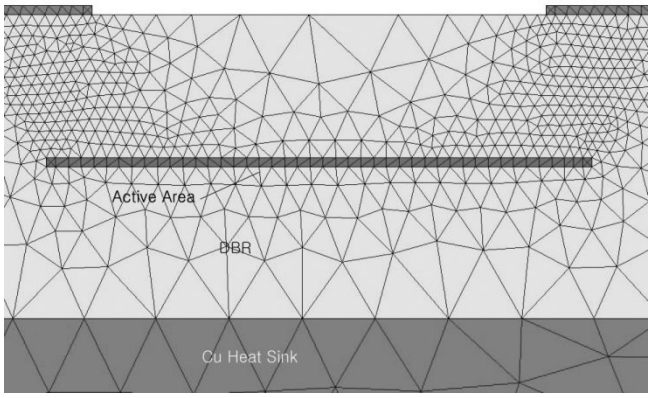


Fig. 5. VCSEL Cooling structures. (a) 250-μm-thick copper block or thermal paste. (b) 30-μm-thick electroplated copper film.

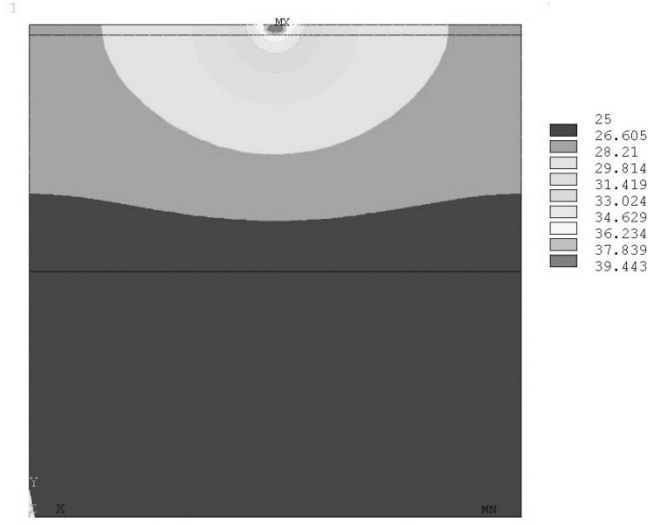
However, the heat generated due to the DBR is relatively small compared to the active region, therefore we ignored this term in our simulation [7]. The heat generation rate in active region (circular shape, diameter of 18 μm) is based on measured value which is 20 mW per VCSEL.

We compared two different cooling structures as depicted in Fig. 5. One is a 250-μm-thick bulk copper as a conductive material and one is a 30-μm-thick electrodeposited copper film. We chose the 30-μm-thick copper film as a heat sink because this is the thickness of the copper trace in the electrical layer of the PCB. The copper film was directly electrodeposited on the n-contact metal pad of the VCSEL array during the electroplating step. The bottom surface of the copper block is maintained at 25 °C.

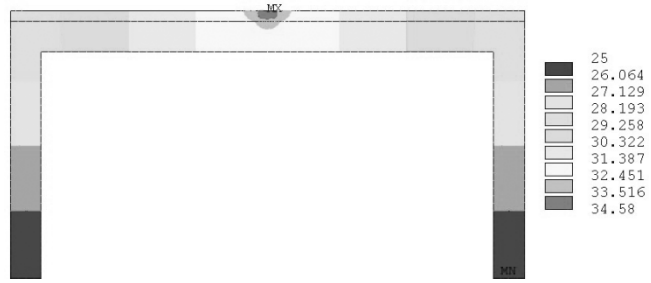
The simulation results are shown in Fig. 6. Fig. 6(a) is the generated mesh profile. For the 250 μm thick copper heat sink block, the temperature at the active region reached 39.4 °C corresponding to a thermal resistance of 722 K/W [see Fig.6 (b)]. For the case of a 30-μm-thick electrodeposited copper film heat



(a)



(b)

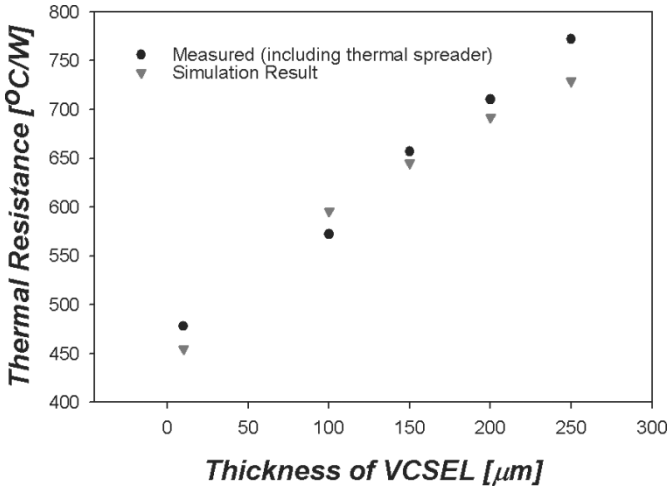


(c)

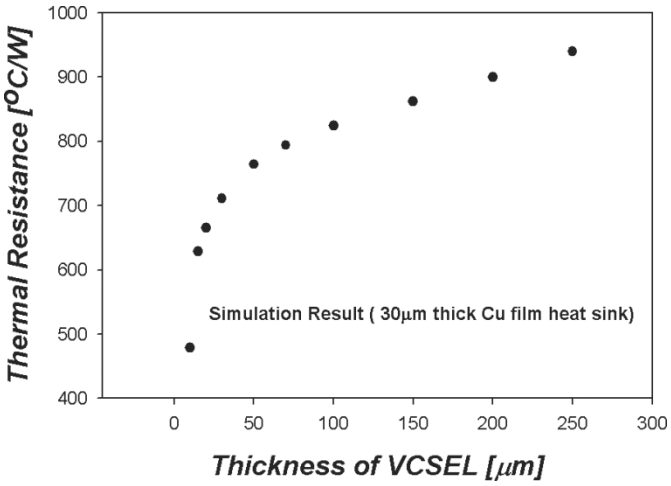
Fig. 6. Two-dimensional (2-D) finite-element analysis results. (a) Generated mesh; (b) 250-μm-thick copper block, 250-μm-thick VCSEL, $\theta_{jc} = 39.4$ °C; (c) 30 μm electroplated copper film, 10-μm-thick VCSEL, $\theta_{jc} = 34.6$ °C.

sink, the junction temperature reached 34.58 °C as in Fig. 6(c) corresponding to thermal resistance of 455 K/W. The higher junction temperature reduces the quantum efficiency and causes catastrophic failure of the device. Despite of lower thermal resistance of the 250-μm-thick copper heat sink block, this structure is not realistic in a fully embedded structure due to difficulty in producing this thickness.

The measured and calculated thermal resistances of the devices are summarized in Fig. 7(a) and (b). As shown in Fig. 7(a), the calculated thermal resistances of the devices are well matched with the measured results. According to this



(a)



(b)

Fig. 7. (a) Measured device thermal resistances as a function of device thickness. (b) Calculated thermal resistances as a function of device thickness for a buried VCSEL with a 30-μm-thick electroplated Cu-film heat sink.

result, the simulation model and process were properly carried out. Fig. 7(b) shows theoretically determined thermal resistances for VCSELs with various thicknesses. For a 30-μm-thick electroplated copper film, the junction temperatures were theoretically determined to be 43.8, 43, 42.2, 41.5, 40.2 and 34.6 °C for 250-, 200-, 150-, 100-, 50-, and 10-μm-thick VCSEL, respectively. The substrate removed VCSEL having a total thickness of 10 μm shows superior optical and thermal characteristics.

V. Summary

The thermal resistance of a fully embedded VCSEL in a board level optical interconnect has been calculated using a two-dimensional finite-element method and validated by comparing with measured thermal resistance values. Directly electroplated copper film was verified as a simple and effective heat sink in the fully embedded structure. The substrate removed VCSEL had the lowest thermal resistance and the best quantum efficiency when compared with the thicker ones out of the same wafer. Employing thin VCSELs in embedded optical interconnects provides a simple packaging strategy and solves thermal related issue.

REFERENCES

[1] B. Lunitz, J. Guttmann, H. P. Huber, J. Moisel, and M. Rode, "Experimental demonstration of 2.5 Gbit/s transmission with 1 m polymer optical backplane," *Electron. Lett.*, vol. 37, no. 17, 2001.

[2] F. Mederer, R. Jäger, H. J. Unold, R. Michalzik, K. J. Ebeling, S. Lehmacher, A. Neyer, and E. Griese, "3-Gb/s data transmission with GaAs VCSEL's over PCB integrated polymer waveguides," *IEEE Photon. Technol. Lett.*, vol. 13, no. 9, Sept. 2001.

[3] D. Krabe, F. Ebling, N. Amdt-Staufenbiel, G. Lang, and W. Scheel, "Electrical optical circuit board built for SMT manufacturing," *Electronic Packaging and Production*, pp. 38–47, July 2000.

[4] E. Griese, "Parallel optical interconnects for high performance printed circuit boards," in *Proc. the 6th Int. Conf. on Parallel Interconnects (PI'99)*, pp. 173–183.

[5] R. T.T. Chen, L. Lin, C. Choi, Y. J. Liu, B. Bihari, L. Wu, S. Tang, R. Wickman, B. Picor, M. K. Hibbs-Brenner, J. Bristow, and Y. S. Liu, "Fully embedded board level guided-wave optoelectronic interconnects," *Proc. IEEE*, vol. 88, pp. 780–793, June 2000.

[6] Y.-C. Lee, S. E. Swirhun, W. S. Fu, T. A. Keyser, J. L. Jewell, and W. E. Quinn, "Thermal management of VCSEL-based optoelectronic modules," *IEEE Trans. on Comp., Packag. Manufact. Technol.*, vol. 19, pp. 540–547, Aug. 1996.

[7] R. Pu, C. W. Wilmsen, K. M. Geib, and K. D. Choquette, "Thermal of VCSEL's bonded to integrated circuits," *IEEE Photon. Technol. Lett.*, vol. 11, pp. 1554–1556, Dec. 1999.

[8] T. Yao, "Thermal properties of AlAs/GaAs superlattices," *Appl. Phys. Lett.*, vol. 51, pp. 1798–1800, 1987.

[9] J. Piprek, T. Tröger, B. Schröter, J. Kolodzey, and C. S. Ih, "Thermal conductivity reduction in GaAs-AlAs distributed Bragg reflectors," *IEEE Photon. Technol. Lett.*, vol. 10, no. 1, Jan. 1998.

[10] C.-K. Lin, S.-W. Ryu, and P. D. Dapkus, "High-performance wafer-bonded bottom-emitting 850 nm VCSEL's on undoped GaP and saphire substrates," *IEEE Photon. Technol. Lett.*, vol. 11, no. 12, Dec. 1999.

[11] H. Fathollahnejad, D. L. Mathine, R. Droopad, G. N. Maracas, and S. Daryanani, "Vertical-cavity surface emitting lasers integrated onto silicon substrates by PdGe contacts," *Electron. Lett.*, vol. 30, no. 15, July 1994.

[12] A. Ghiti, M. Silver, and E. P. O'Reilly, "Low threshold current and high differential gain in ideal tensile and compressive strained quantum well lasers," *J. Appl. Phys.*, vol. 35, pp. 4626–4628, 1992.

[13] G. Belenky, C. L. Reynolds Jr., L. Shterengas, M. S. Hybertwsen, D. V. Donetsky, G. E. Shtengel, and S. Luryi, "Effect of p-Doping on the temperature dependence of differential gail in FP and DFB 1.3-mm InGaAsP-InP multiple-quantum-well lasers," *IEEE Photon. Technol. Lett.*, vol. 12, Aug. 2000.

Chulchae Choi, photograph and biography not available at the time of publication.

Lei Lin, photograph and biography not available at the time of publication.

Yujie Liu was born in Sichuan, China, in 1974. She received the B.S. and M.S. degrees in electronic science from Nankai University, Tianjin, China, in 1995 and 1998, respectively. She is currently working toward the Ph.D. degree in electrical engineering at the University of Texas at Austin.

Her area of research is in guided-wave optical interconnects.

Ray T. Chen (M'91–SM'98) is the Temple Foundation Endowed Professor in the Department of Electrical and Computer Engineering at the University of Texas (UT) at Austin. His research group has been awarded more than 60 research grants and contracts from such sponsors as the Department of Defense, the National Science Foundation, the DOE, NASA, the State of Texas, and private industries. The research topics include guided-wave and free-space optical interconnects, polymer-based integrated optics, a polymer waveguide amplifier, graded index polymer waveguide lenses, active optical backplanes, traveling-wave electroptic polymer waveguide modulators, optical control of phased array antenna, GaAs all-optical crossbar switch, holographic lithography, and holographic optical elements. The optical interconnects research group at UT Austin has reported its research in more than 250 published papers. He has served as a consultant for various federal agencies and private companies and delivered numerous invited talks to professional societies.

Dr. Chen is a Fellow of the The International Society for Optical Engineers (SPIE) and of the Optical Society of America (OSA). He is a Senior Member of the IEEE Lasers and Electro-Optics Society (LEOS) and a Member of PSC. He has chaired or has been a program Committee Member for more than 40 domestic and international conferences organized by SPIE, OSA, IEEE, and PSC.