Thin film optical waveguide and optoelectronic device integration for fully embedded board level optical interconnects

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ABSTRACT

We demonstrate a flexible optical waveguide film with integrated Vertical-cavity surface-emitting laser (VCSEL) and positive-intrinsic-negative (PIN) photodiode arrays for fully embedded board level optical interconnects. The optical waveguide circuits with 45° micro-mirror couplers are fabricated on a thin flexible polymeric substrate by soft molding. 45° micro-mirrors on waveguide array for fully embedded board level optical interconnections are investigated both theoretically and experimentally. Smooth mirror surface fabrication is demonstrated by using microtome blade. Thin film VCSEL arrays and PIN photodiode arrays are directly integrated on to the waveguide film. Measured propagation loss of the waveguide was 0.3dB/cm at 850nm.

Keywords: optoelectronic interconnects, waveguide, soft molding, VCSEL, micro-mirror coupler, PDMS, SU-8

1. INTRODUCTION

The speed and complexity of integrated circuits have increased rapidly in recent years, and this trend continues. As the number of devices per chip, the number of chips per board, the modulation speed, and the degree of integration continue to increase, electrical interconnects are facing their fundamental bottle-necks, such as speed, packaging density, fan-out, and power dissipation. Multichip module (MCM) technology is employed to provide higher data transfer rates and circuit densities [1]. However, the state-of-art technologies based on electrical interconnects fail to provide the required multi-Gbit/s clock speed and communication distance in intra-MCM and inter-MCM hierarchies [2]. Even if the transmission speed was left the same and data bus width expanded, it would probably mean more IC pins and other more interconnect layers problems [3]. Optical interconnect is a promising solution to overcome the electrical interconnect bottleneck problems since it has inherent advantages of high bandwidth, no capacitive loading and immunity to electromagnetic interference. In contrast to a electrical interconnect, the optical interconnection transmits information at a higher data rate, consumes less power, and occupies less real estate on the board. Recently many research groups have worked on board level optical interconnect systems and demonstrated their viability [4]-[6]. However, there are still some difficulties in packaging and manufacturing to overcome.

In this report we propose employing fully embedded optical interconnects (FEOI) at the printed circuit board (PCB) level, in a reliable and robust fashion. FEOI provide not only process compatibility with the standard PCB processes but also provide a reduced footprint on the PCB. This is accomplished by fully embedding all optical components such as light sources, channel waveguides and detectors among the other PCB electrical layers as indicated in Fig 1. The pulsed laser light from the VCSEL is normally coupled into the multimode waveguide through a 45° micro-mirror coupler. It propagates through the waveguide, then is reflected at the output interface of the waveguide by another 45° micro-mirror coupler, and finally is illuminated vertically on the active area of the photodetector. This process provides no interface problem between electronic and optoelectronic components as conventional approaches do, and additionally, real estate of the PCB surface is free to be occupied by electronics and not by optoelectronic components. The performance enhancement due to the employment of the optical interconnection is observed. In order to implement FEOI; the characteristics of four main components have to be investigated.

- thin film vertical cavity surface emitting laser (VCSEL) as optical transmitter
- flexible polymer waveguide as optical transmitting media

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- 45° micro-mirror couplers
- thin film PIN photodiode as optical receiver.

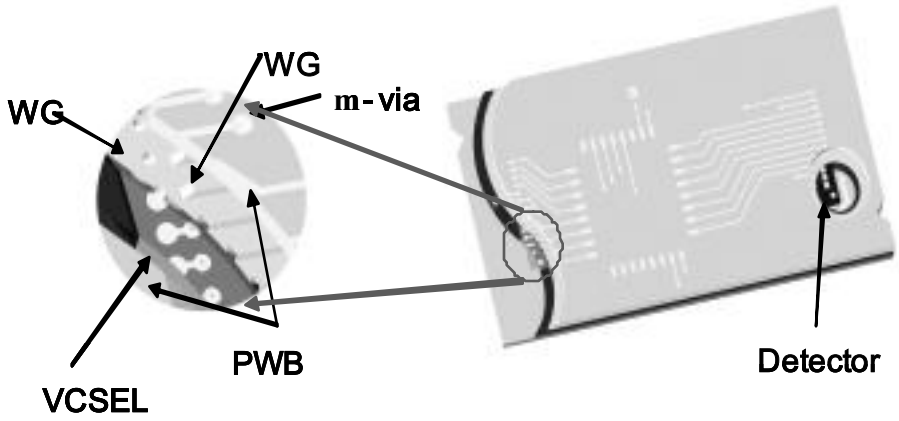


Fig. 1. Illustration of a fully embedded board level optical interconnect

2. POLYMER WAVEGUIDES

Polymer-based waveguides are employed in this FEOI to provide the integrated optical circuitry. Polymers have exclusive advantages for use as optical layer waveguide on PCB. They provide ease of process, cost-effectiveness and high performance characteristics such as lower optical loss and thermal stability [1]. For integration of polymer waveguides into multi-layer PC boards to occur, the waveguides have to withstand more than 1 hour exposure of 180ºC and 350psi during the lamination. For this reason, the ultra-violet (UV) curable resin ZPU12-460 and ZPU12-450 (available by Zen Photonics) were chosen as the core and cladding materials. The refractive index of ZPU12-460 and ZPU12-450 are 1.47 and 1.46 at 850 nm. They are low loss, low birefringence and environmental stable. The polymeric foil Topas (cyclo-olefin-copolymer) from Ticona was chosen as the mechanical support for optical layer. The Topas film is highly transparent, has a low loss at 850nm and has a high glass transition temperature (150°C).

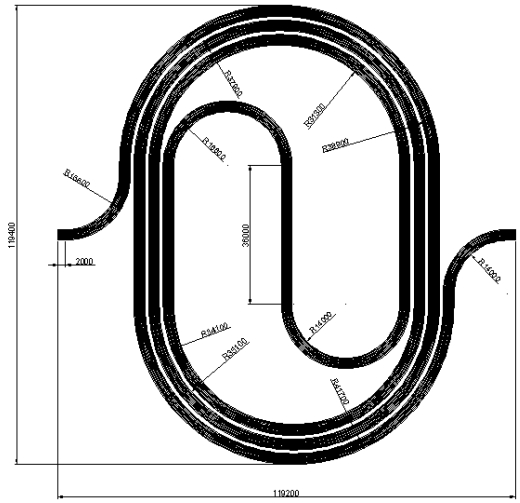


Fig. 2. The total length of 109 cm waveguide layout design

For board-level interconnection, the interconnection distance can be easily in the range of tens of centimeters up to 1 meter. We designed the two waveguide patterns: a 51 cm long and a 109 cm long pattern shown in Fig.2. Both had cross

sections of 50μm×50μm to relax alignment tolerances and contained 12 waveguide channels with 250μm separation between individual channels.

We fabricated the channel waveguides using the soft molding technique (micro transfer molding), which can transfer a pattern with feature sizes greater than 30nm easily on to a substrate using an elastomer mold. In the soft molding process, we first drop liquid prepolymer on the patterned structure of the PDMS mold and then place the filled mold in contact with the substrate. After the prepolymer is cured by UV irradiating, the polydimethylsiloxane (PDMS, Sylgard 184 kit, Dow Corning) mold is peeled away to leave the waveguides on the surface of the substrate. Compared with photolithography, reactive ion etch (RIE) and laser direct-writing, soft molding has the following advantages:

- Long and thick waveguide array can be made with simple equipment.
- Since PDMS is flexible and has low interfacial free energy, it is easy to be released from the mold even if the mold area is large.
- Soft molding allows the fabrication of a waveguide on any type and size of substrates.
- Soft molding can make three-dimensional structures including the waveguide array and micro-mirror coupler in one single step.
- Lastly, soft molding is low cost and suitable for mass production.

Our procedures for fabricating waveguides using soft molding consist of three steps as shown in Fig. 3: (1) fabrication of master waveguide structure, (2) Fabrication of PDMS mold, and (3) Waveguide fabrication. We will explain each step in details.

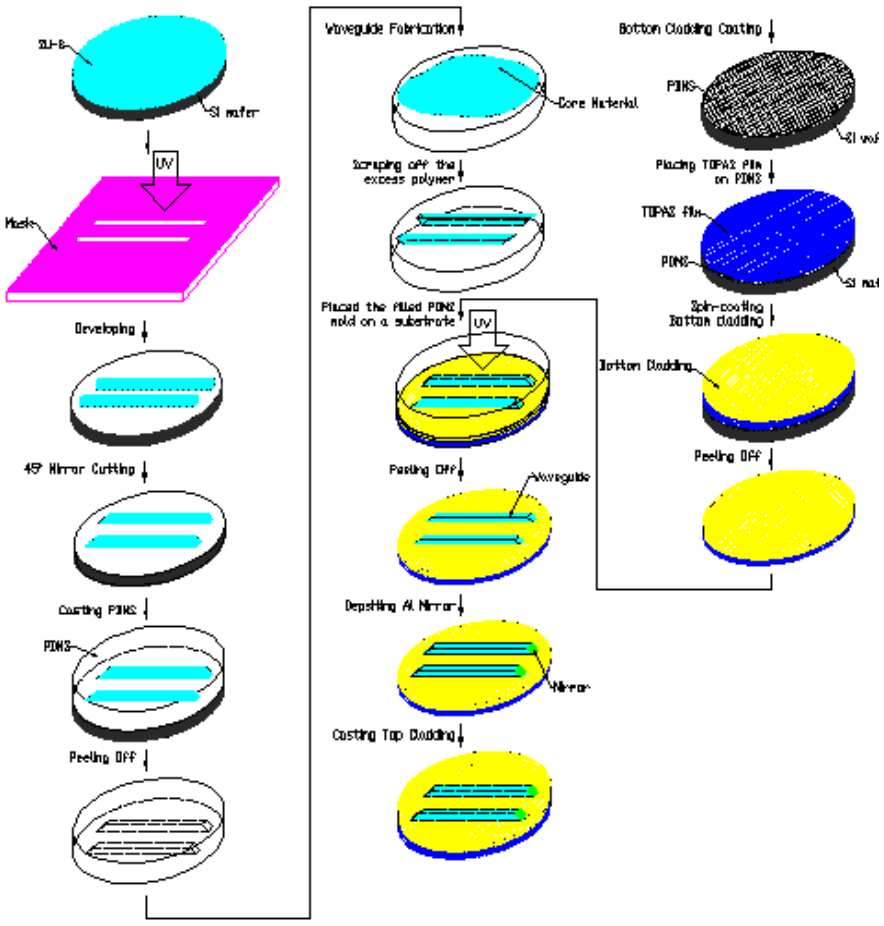


Fig. 3. Schematic diagram of the waveguide fabrication using soft molding

1. Fabrication of Master Waveguide Structure.

The master waveguide structure is made on the silicon wafer using photolithography. The procedure mainly consists of **six sub-steps:**

(1) Substrate Cleaning. To improve the adhesion of SU-8 film on the substrate, the silicon wafer was first cleaned by a piranha solution (H_2SO_4: H2O2=2:1) and then dehydrated on a hot plate at 200° C for 5min.
(2) Coating and Pre-baking. A 50-μm-thick SU-8 (MicroChem Corp.) film was spin coated on the six-inch silicon wafer and pre-baked at 65°C for 30min followed by 90°C for 30min on the hot plate with 30° C/h ramping rate. After the bake, we cooled down SU-8 film slowly at room temperature.
(3) Exposure. The SU-8 film was then exposed using a Karl Suss mask aligner with the exposure dose of 220mJ/cm^2. T-toping phenomena were successfully corrected by filtering out ultraviolet radiation below 350nm. A straight and smooth sidewall profile (Fig. 4) was formed allowing for easy removal of the PDMS mold from the waveguide structure.
(4) Post exposure bake. The film was post exposure baked on the hot plate at 65° C for 1min and 90° C for 2min.
(5) Develop. The wafer with SU-8 film was placed into the SU-8 developer (PGMEA) for 3min to remove the unexposed resist.
(6) To get 45° micro-mirror couplers, the master waveguide structure is put on a 45° tilted stage and cut both end by the commercial blade. During cutting process, the waveguide is heated to glass transition temperature so as to achieve smooth cutting surface and avoid cracking or peeling off.

2. Fabrication of PDMS mold.

(1) The PDMS material is composed of two parts, the base and the curing agent. They were mixed at a ratio of 10: 1 and were degassed under vacuum to eliminate air bubble.
(2) Pour un-polymerized PDMS onto the patterned silicon wafer, cure it on hot plate at 60°C for 12 hours, and peel the PDMS mold off the silicon wafer. The waveguide patterns with 45° micro-mirror couplers are transferred from the master waveguide structure to the PDMS mold. The PDMS mold can reproduce features up to within a few nanometers from the master.

3. Waveguide Fabrication.

(1) A drop of UV curable resin ZPU12-RI-460 (Zen Photonics) is applied on the patterned structure of the PDMS mold and excess resin is scraped off.
(2) A bottom cladding coating is applied by firstly spin coating a 20 μm layer of PDMS pre-polymer on the silicon wafer and curing it on the hot plate at 90° C for 1min. The TOPAS film is then placed on the PDMS layer using a technique that starts at one side of the wafer and then gradually works to the other side ensuring that air bubbles are not trapped between TOPAS film and PDMS support layer. Next, a 20μm layer of ZPU12-RI-450 (Zen Photonics) is spin coated on to the TOPAS film. After UV exposure for curing, the TOPAS film is removed from the PDMS support layer.
(3) The TOPAS film (now with a 20μm layer of ZPU12-RI-450 as its bottom layer) is pressed onto the filled PDMS mold.
(4) The pre-polymer ZPU12-RI-460 is cured by UV irradiating until fully cured. Then the PDMS mold is peeled off, leaving the waveguide array. PDMS is a good choice for the mold material because it is transparent to the UV light used to cure the prepolymer. The PDMS mold can be used for multiple replication cycles without any damage.
(5) The waveguides are coated in a N_2 blanket while baked in an oven at 160° C for 30min.
(6) The surfaces of the 45° micro-mirrors are deposited with aluminum (Al) to ensure the total internal reflection.
(7) ZPU12-RI-450 is coated on the waveguide as the top cladding.

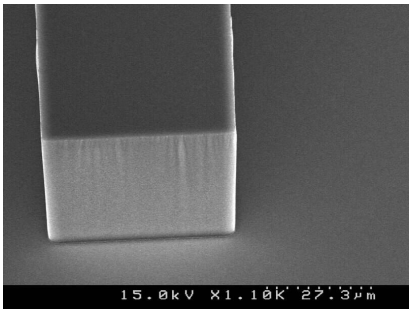


Fig. 4. SEM image of a typical SU-8 pattern using photolithography

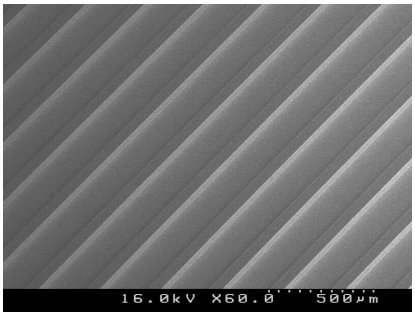


Fig. 5. SEM image of a waveguide array using soft molding

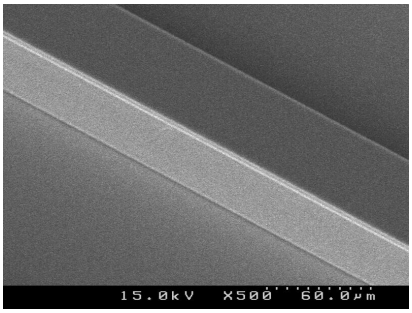


Fig. 6. SEM image of straight and smooth sidewall of a molded waveguide

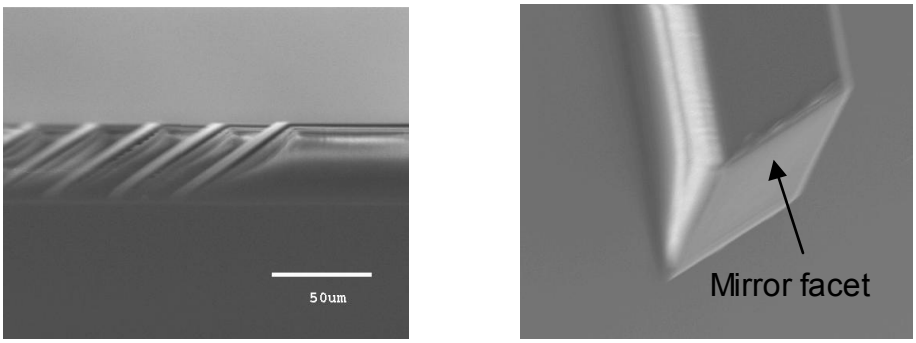
The results are shown in Fig. 5 with the channel waveguides having 50µm × 50µm cross-sections fabricated by soft molding. Fig. 6 shows the straight and smooth sidewall of the molded waveguides. The residual layer where the mold is contact with the substrate can be controlled to be less than 1µm by reducing the prepolymer applied on the PDMS mold. In experiments using this technique, optical loss was measured by the cut-back method. The 850nm VCSEL light was butt-coupled to the waveguide by using a 50/125µm graded index (GI) multimode fiber and the output light was then butt-coupled to photo detector by using a 62.5/125µm graded index (GI) multimode fiber. The measured propagation loss was 0.3dB/cm at 850nm wavelength.

3. 45° WAVEGUIDE COUPLERS

To efficiently couple optical signals from vertical cavity surface emitting lasers (VCSEL) to polymer waveguides and then from waveguides to photo-detectors, two types of waveguide couplers are investigated. They are tilted grating couplers and 45^{o} waveguide mirrors. There are a large number of publications in grating design [10] - [14]. However, the surface-normal coupling scenario in optical waveguides has not been carefully investigated so far. The profile of tilted grating greatly enhances the coupling efficiency in the desired direction. A very important aspect of manufacturing of such coupler is the tolerance interval of the profile parameters, such as the tooth height, the width and the tilt-angle. However the tilted grating coupler has inherent wavelength sensitivity and is not applicable for planarized waveguide.

The second method of waveguide coupling is through the total internal reflection (TIR). Such the 45^{o} waveguide mirror is relatively insensitive to the wavelength of light and has high coupling efficiency. There are various techniques to fabricate 45^{o} mirror such as laser ablation [15], oblique reactive ion etching (RIE) [1], temperature controlled RIE [16], re-flow [17] and machining [18]. The laser ablation method is subjected to lower throughput and surface damage. The oblique RIE method is limited by directional freedom. The temperature controlled RIE method is free from directional freedom but the quality of the mirror depends on process and materials. The re-flow method is also subjected to lower throughput. The machining provides good surface profile; however, it is difficult to cut individual waveguide on a substrate due to the physical size of the machining tool. We developed a new fabrication method using a commercial blade. This method is simple and cost-effective.

The wafer is put on a 45 degree tilted stage, with position adjustable, while the blade can only be moved horizontally, which will ensure accuracy of the angle. During cutting process, the waveguides are heated, thus the cutting surface will be smoother and waveguide cracking may be avoided. The side-off view and surface of mirror is show in Fig. 7. After the waveguides are fabricated by molding method, 45° surfaces are already formed for every single waveguide.



(a) (b)

Fig. 7 (a) SEM image of the waveguide with 45° micro-mirrors
(b) Enlarged view of the mirror surface

The coupling efficiency of the micro-mirror is one of the most critical issues in the fully embedded optical interconnects. Higher coupling efficiency between waveguide and VCSEL or photo detector is desirable to achieve low power dissipation, low bit error rate (BER) and high-speed performance. We assume that the distribution of the VCSEL is Gaussian profile and lights within acceptance angle of waveguide are totally coupled into the waveguide. The substrate thickness (bottom cladding) and the aperture of the VCSEL are 127μm and 12μm, respectively. There are about 10 supporting modes in the 50μm × 50μm waveguide with the refractive index difference Δn=0.01. For an exact calculation, we have to consider all the modes, but the number of mode is quite large. It can be treated as geometrical optics [19].

The coupling efficiency, η, can be calculated by the ratio of coupled power to total laser power.

$$\eta = \frac{\int_{-r_c}^{r_c} |E(r,z)|^2 dr}{\int_0^{\infty} |E(r,0)|^2 dr} = \left(\frac{\omega_0}{\omega(z)}\right)^2 \int_{-r_c}^{r_c} |E(r,z)|^2 dr$$

where, r_c is the maximum radius at the mirror facet which correspond to the acceptance angle of the waveguide. Fig. 8 shows the intensity distributions of laser light at the mirror surface, and the coupling efficiencies as a function of angular deviation from 45°.

The facet of 45° mirror was coated with the aluminum to ensure the reflection because TIR (total internal reflection) does not occur due to the top cladding layer. The reflectance of the aluminum is about 92%. In this scheme all laser lights fall within the mirror. The coupling efficiency is 92% which means nearly 100% of the light is coupled into the waveguide excluding the reflectance due to aluminum. Fig. 8 (b) shows the input coupling efficiency as a function of angular deviation from 45°. The input coupling efficiency is higher than 90% when the mirror angle is within 45° ± 1.5°.

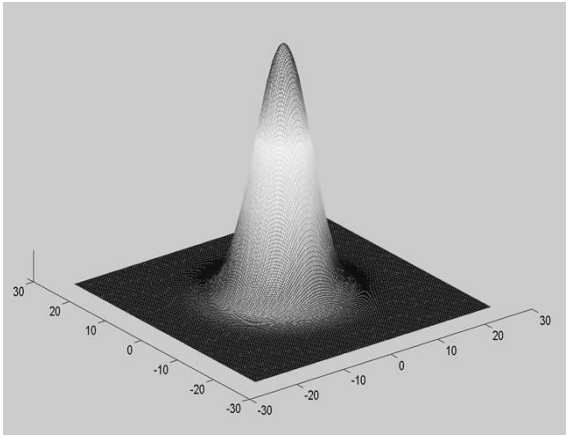


Fig. 8 (a). Intensity distributions at the mirror surface

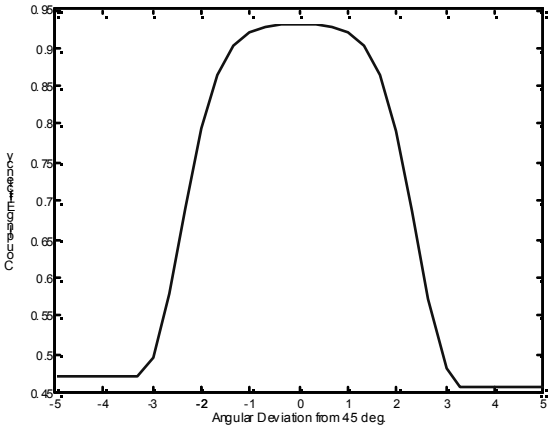


Fig. 8 (b). Coupling efficiency versus the angular misalignment

When the light coupled out from the micro-mirror coupler reaches the photo detector, it will propagate in the bottom cladding layer for a distance of about one hundred microns. The output profile from the 45° micro-mirror coupler can be determined using diffraction theory. According to Fourier Optics [20], the near field distribution is given by

$$U(x,y,z)=\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty}A\left(\frac{\alpha}{\lambda},\frac{\beta}{\lambda},0\right)\exp\left(j\frac{2\pi z}{\lambda}\sqrt{1-\alpha^2-\beta^2}\right)\exp\left\{j2\pi\left(\frac{\alpha}{\lambda}x+\frac{\beta}{\lambda}y\right)\right\}d\frac{\alpha}{\lambda}d\frac{\beta}{\lambda}$$

where *U(x, y, z)* is the complex amplitude of the observed field at point *(x , y, z*), and *z* the distance from the upper surface of the 45° micro-mirror coupler to observing point, and the angular spectrum of the distribution U(x, y, 0) is

$$A\left(\frac{\alpha}{\lambda},\frac{\beta}{\lambda},0\right)=\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty}U(x,y,0)\exp\left\{-j2\pi\left(\frac{\alpha}{\lambda}x+\frac{\beta}{\lambda}y\right)\right\}dxdy$$

The theoretical output profiles at z = 50 μm, 100 μm and 1000μm from the 45° micro-mirror coupler are shown in Fig. 9 (a)-(c), respectively [21]. If the photodetectors are mounted close to the micro-mirror couplers, then most light of light can reach the photodetectors and thus the waveguide-to-detector coupling efficiency can be very high.

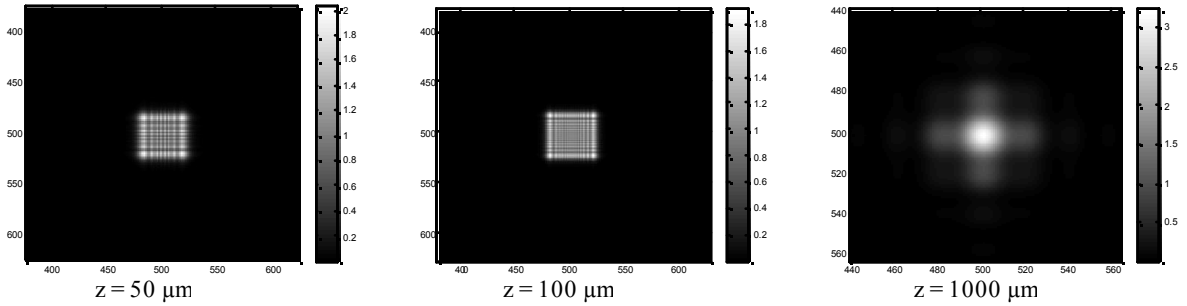


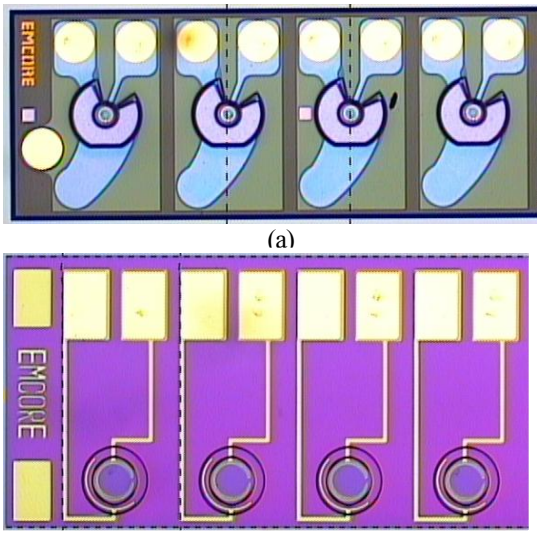
Fig. 9. Diffraction patterns of the output light from the micro-mirror coupler at the distance z = 50, 100, and 1000 μm

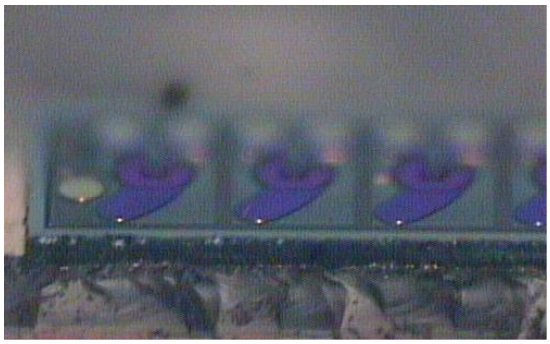
4. VCSELS AND PIN PHOTODIODE

The VCSEL emitting 850nm wavelength light is the most suitable source because manufacturing technology of 850nm VCSEL is matured and relatively cheap. Compared to edge-emitting lasers, VCSEL offers a very low threshold current with much less temperature sensitivity, moderate optical power, very high direct modulation bandwidth, wide operating temperature range, and ease of packaging in an array configuration due to the unique surface-normal output nature.

MSM photodetectors have been widely used for optical interconnection due to their ease of integration with the IC processes. Since their inception, MSM detectors have been mainly used for laboratory research. However, as stated in [22], "the telecommunication industry has long adopted PIN PDs for their higher responsivity, and only few commercial 10GHz MSM PDs are available, and there are no commercially available 10 Gb/s transimpedance amplifier (TIA) designed for MSM. It will be a great cost reduction to use the current manufacture capacity of PIN PDs to integrate high speed optical interconnects." Based on overall performance, we choose the low cost and commercial available 1 × 12 PIN photodiode array as optical receiver for fully embedded optical interconnection.

A very thin VCSEL and PIN photodiode are needed in a fully embedded board level optical interconnects because they are buried between the optical layer and the electrical layers. The original 200 μm thickness GaAs substrate of the VCSEL and PIN photodiode is removed by CMP (Chemical Mechanical Polishing) process. The final thickness of substrate removed VCSEL and PIN photodiode was around 10 μm. Fig. 10 (a) shows a section of the 12-channel VCSEL and Fig. 10(b) shows a section of the 12-channel PIN photodiodes and Fig. 10 (c) shows the 10 μm thin VCSEL array where the substrate is removed.





(c)

Fig. 10 (a) A SEM picture of 4 elements of 1× 12 GaAs VCSEL array. (b) 4 elements of 1× 12 GaAs PIN photodiode array. (c) substrate removed 10 µm thin VCSEL array

Output laser power and voltage versus current characteristics of 10 µm thick VCSEL are measured, and the result is shown in Fig. 11. Threshold current and threshold voltage were 0.7mA and 1.5 V, respectively. Electrical characteristics of 10 µm thickness PIN photodiode were measured shown in Fig. 12. At reverse bias condition from 1 volt to 5 volt, dark current of 10 µm thick PIN photodiode was around 0.7nA. After polishing to its final thickness, there is no significant change in optoelectrical characteristics.

Frequency response and eye-diagram of 10 µm thick VCSEL were measured using a network analyzer (HP 8703A) and a digital communication analyzer (HP 83480A), respectively. Eye-diagram measurements have been carried out with a PRBS-NRZ mode of 2^{31}-1 word-length at a data rate of 10 Gbps (applied bias: 5mA / 1.9 V, amplitude: 0.5mA). Fig. 13 shows the eye was wide open and measured Q-factor and jitter-RMS values were 5.18 and 4.6ps, respectively. The 3 dB-bandwidth of the 10 µm thickness VCSEL was extended up to 10 GHz at 5mA bias condition as shown in Fig. 14.

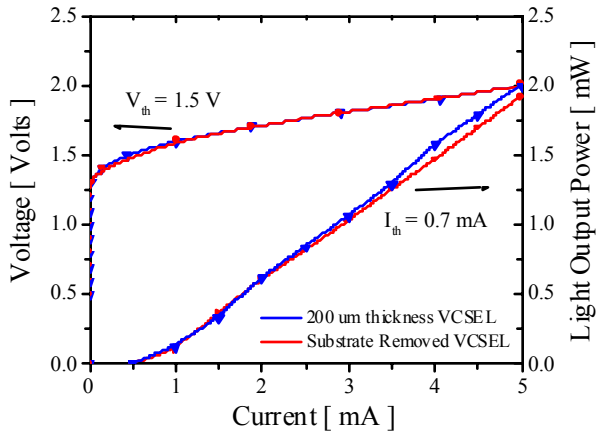


Fig. 11 The L-I-V curves of 10 µm thick VCSEL array

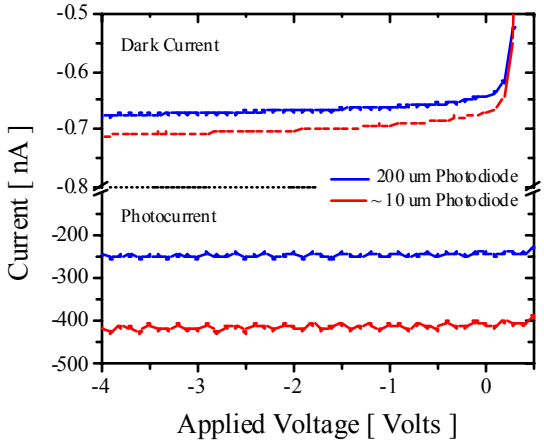


Fig. 12 The I-V curves of 10 µm thick PIN photodiode array

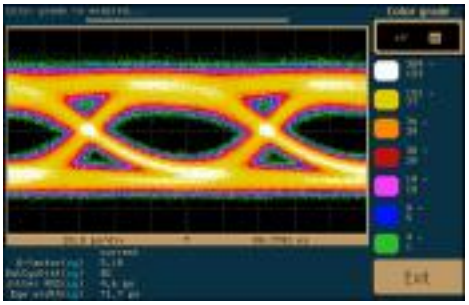


Fig.13 VCSEL eye at 10 Gb/s

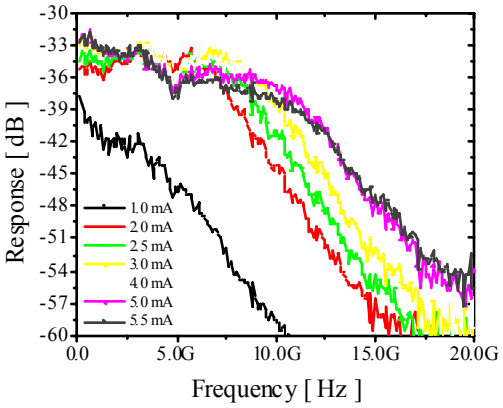


Fig.14 Frequency response of the VCSEL array

5. THERMAL MANAGEMENT OF THE BURIED VCSEL

The substrate of VCSEL was removed; very thin VCSEL (~10 μm) enables the formation of the fully embedded optical interconnection, as depicted in Fig.1. However, VCSEL in this embedded scheme was surrounded with thermal insulator such as polymer waveguides and bonding film; therefore, generated heat builds up within the embedded layer. The improper heat dissipation can lead to thermal runaway. The increasing temperature leads wavelength shift, increasing a threshold current, reducing quantum efficiency, shorten device life time, and dissipating more power. The embedded VCSEL cannot be replaced after integration. Therefore, the effective heat removal of the VCSEL array is a critical issue in the fully embedded structure.

To be compatible with PC board technology, we use an n-contact metal affiliated with the bottom DBR mirror of the VCSEL die as a heat spreader, and a part of the heat sink by directly electroplating with copper during the integration process. In general, thermally conductive paste (usually contains fine metal flakes) was used for low power laser diode packaging. In a high power laser diode packaging, the gold-tin (Au-Sn) eutectic alloy was used to bond LD on heat sink. The thermally conductive paste has a ten times smaller thermal conductivity than that of copper. Therefore, thermally conductive paste can not be used because it has a lower thermal conductivity than copper. Usually several tens of micrometer thick copper was deposited in copper contained acid chemical solution during PCB process. It can be used as a very good electrical and thermal passage, simultaneously. The thermal resistance of a buried VCSEL depends on the device structure and the packaging structure. Once the device was designed there is no other ways to change thermal resistance of the device. The direct bonding of the device using Cu electroplating reduces thermal resistance of the device due to the absence of the lower thermal conductivity bonding epoxy [23].

For steady state and constant heat generation case, the thermal diffusion equation is

$$k\nabla^2 T + q = 0$$

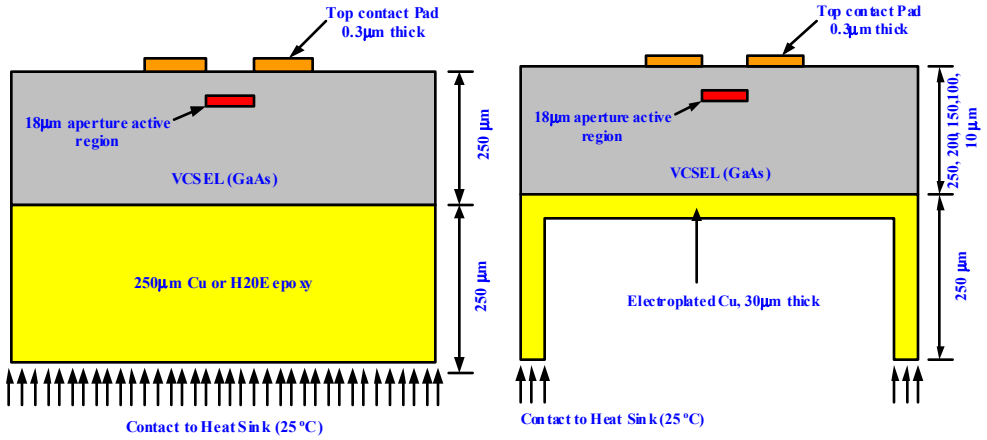
where, T is the temperature, k is the thermal conductivity, and q is the heat generation rate. Once temperature difference (ΔT) between device and heat sink was known, thermal resistance (R_{th}) of the embedded VCSEL can be calculated by

$$R_{th} = \Delta T / \Delta P$$

Here, ΔP is the dissipated power.

ANSYS software was used to perform a 2-D finite element thermal distribution analysis. The thermal conductivities of GaAs, DBR mirror and copper are 4.6 X 10^{-5} W/μm·K, 2.3 X 10^{-5} W/μm·K, and 4 X 10^{-4} W/μm·K, respectively. As VCSEL parameters, active diameter of 18μm and the thickness of 0.3μm, power dissipation of 20 mW were used.

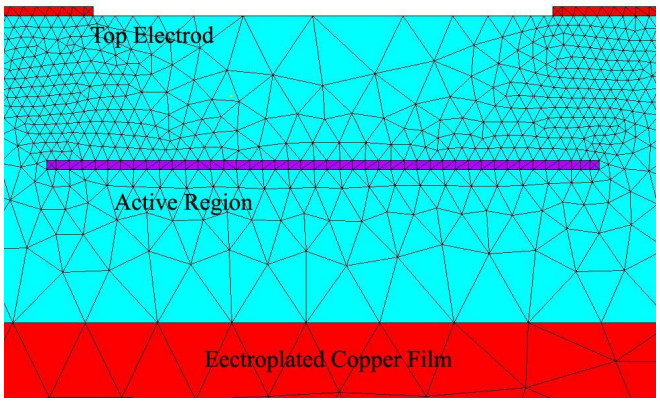
We compared two different cooling structures as depicted in Fig. 15. One is 250µm thick bulk copper as a conductive material (Fig.15 (a)) and one is a 30µm thick electrodeposited copper film (Fig. 15 (b)). To overcome realization of thick heat sink, the electroplated copper foil on the back side of VCSEL was introduced. We chose the 30µm thick copper film as a heat sink because this is the thickness of the copper trace in the electrical layer of the PCB. The copper film can be directly electro-deposited on the n-contact metal pad (Au-Ge/Ni/Au) of the VCSEL array during the electroplating step. The shape of the copper foil heat sink looks like rectangular shape cap. During the simulation the bottom surface of the copper block or thermal conductive paste or copper foil is maintained at 25°C.



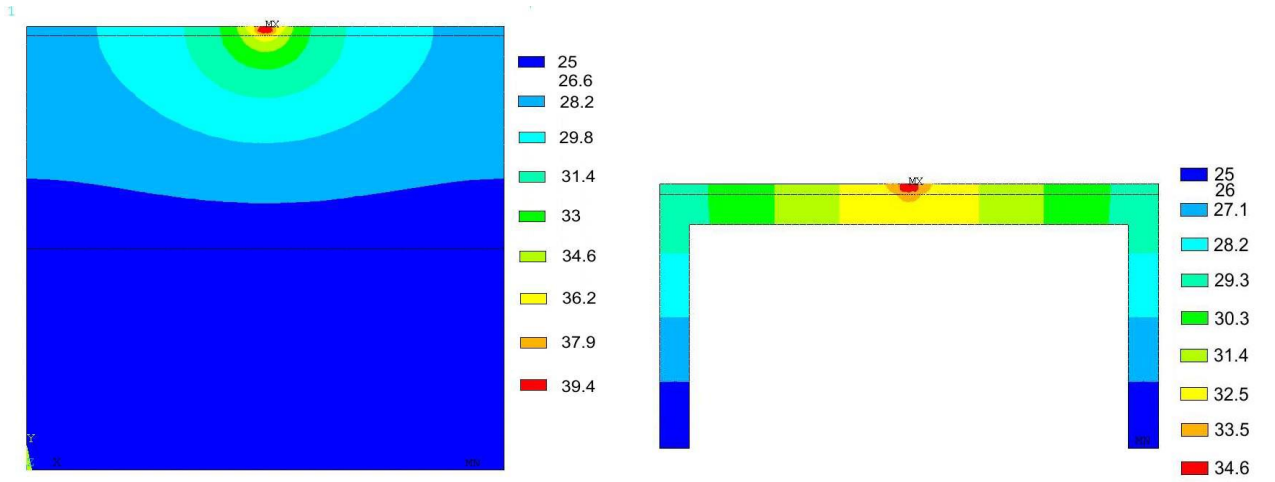
(a) (b)

Fig. 15 Two types of embedded heat sink structure. (a) 250µm thick electroplated copper or thermal conductive paste (H20E™, Epotek), (b) 30µm thick electroplated copper film.

The simulation results are shown in Fig. 16. Fig. 16 (a) is the automatically generated triangular mesh profile. For the 250µm thick copper heat sink block, the temperature at the active region reached 39.4°C corresponding to a thermal resistance of 722K/W (Fig. 16 (b)). For the case of a 30µm thick electrodeposited copper film heat sink, the junction temperature reached 34.58°C as in Fig. 16 (c) corresponding to thermal resistance of 455K/W. The higher junction temperature reduces the quantum efficiency and causes catastrophic failure of the device. Despite of lower thermal resistance of the 250µm thick copper heat sink block, this structure is not realistic in a fully embedded structure due to difficulty in producing this thickness.

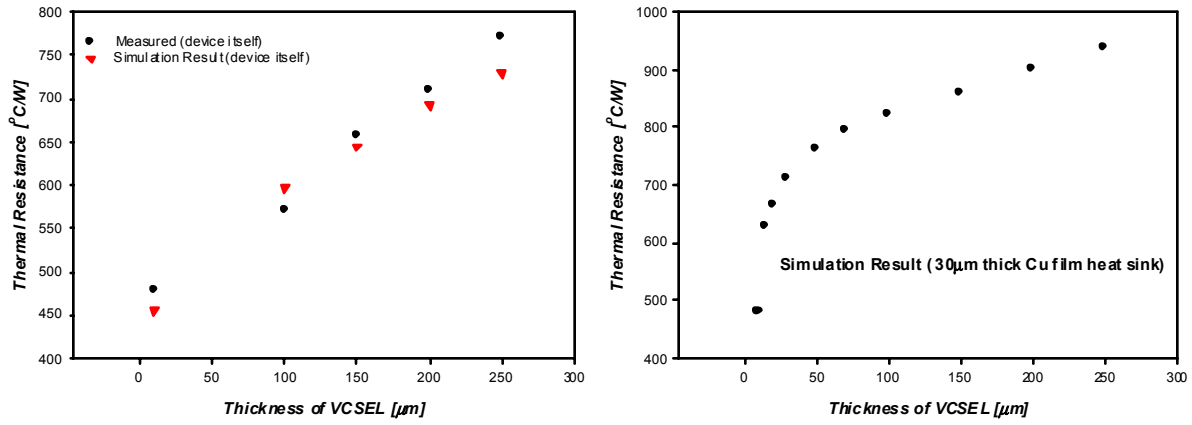


(a)



(b) (c)

Fig. 16. Two-dimensional (2-D) finite-element analysis results. (a) Generated mesh; (b) 250-μm-thick copper block, 250-μm-thick VCSEL, θ_{jc}=39.4°C; (c) 30 μm electroplated copper film, 10-μm-thick VCSEL, θ_{jc}=34.6°C;



(a) (b)

Fig. 17 (a) Measured device thermal resistances as a function of device thickness. (b) Calculated thermal resistances as a function of device thickness for a buried VCSEL with a 30-μm-thick electroplated Cu-film heat sink.

The measured and calculated thermal resistances of the devices are summarized in Fig 17(a) and Fig 17(b). As shown in Fig. 17(a), the calculated thermal resistances of the devices are well matched with the measured results. According to this result, the simulation model and process were properly carried out. Fig. 17(b) shows theoretically determined thermal resistances for VCSELs with various thicknesses. For a 30μm thick electroplated copper film, the junction temperatures were theoretically determined to be 43.8, 43, 42.2, 41.5, 40.2 and 34.6°C for 250, 200, 150, 100, 50 and 10μm thick VCSEL, respectively. The substrate removed VCSEL having a total thickness of 10μm shows superior optical and thermal characteristics.

6. DEVICE INTEGRATION ON FLEXIBLE WAVEGUIDE FILM

The flexible waveguide film will be inserted between electrical circuit layers and laminated with them on the PC board. The driving electrical signals are through micro vias connecting to the surface of the PC board. Figure 18 illustrates device integration process.

(1) Laminate one mil thick copper foil on the top of the flexible waveguide film. The micro vias can not be electroplated without copper foil lamination since the aspect ratio of the thickness of additional electrical layers and the diameter of device pad is large than 100. The aspect ratio of vias is reduced by introducing the copper foil just above the waveguide layer; hence, we can electroplate micro via. Furthermore, the patterns on the copper foils can be bigger. This means that larger registration error can be allowed during laminating process with electrical layers.

(2) This copper foil is patterned to form the top electrical pads for VCSEL and photo-detector.

(3) Micro vias are drilled by UV-Nd:YAG laser.

(4) Optoelectronics device bonding on the flexible film. There are two ways to bond the VCSEL array and PIN photodiode array: UV curable adhesive and melt bonding.

The melt bonding means the devices is heated to the glass transition temperature of the TOPAS film to bond the device on to the film.

The UV curable adhesive bonding was performed on our lab. The integration was performed on Karl-Suss mask aligner. The flexible waveguide film was first bonded on a piece of clear glass wafer. The VCSEL array and PIN photodiode array were placed on the sample holder. Very small amount of UV curable adhesive (Norland Optical Adhesive 61) was applied on the top of the VCSEL array and PIN photodiode array. After the apertures of VCSEL array was aligned with micro-mirror couplers of waveguide, UV curable adhesive was cured by UV exposure. Then the VCSEL array was attached on the TOPAS film. Same aligning procedure was performed on the PIN photodiode array. Fig. 19 shows the integrated VCSEL and PIN photodiode array on a flexible waveguide film.

(5) Electroplating. The flexible waveguide film was submerged in the copper electroplating solution to plate the side walls of the micro vias and device pads. Now the optical interconnection layer is ready to be laminated with the electrical layers on the PC board.

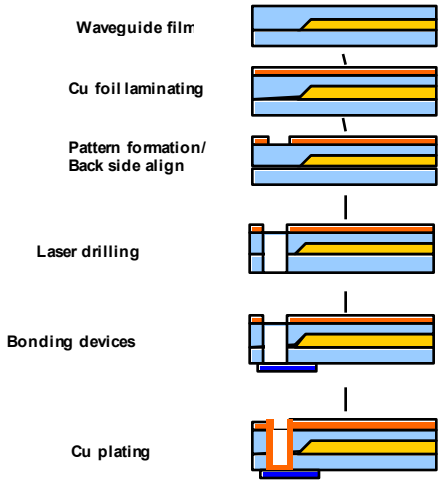


Fig.18 Device integration process flow chart

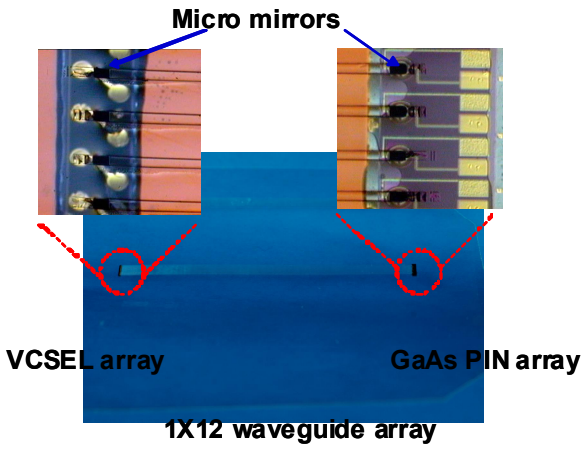


Fig.19 Integrated VCSEL and detector arrays on a flexible optical waveguide film

7. CONCLUSION

Soft molding has been used for fabrication of waveguides with large core sections (50 μm ×50 μm) in areas of over 100 square centimeters with simple equipment. A multimode waveguide array with 45° micro-mirrors was fabricated using

the soft molding process. The measured propagation loss of the waveguides was 0.3dB/cm at 850nm. This proved soft molding is a potential technology for low cost, rapid, and mass production of waveguides in optical interconnections.

The 45° micro-mirror couplers were cut using a microtome blade. The coupling efficiency of aluminum coated micro-mirror was 92%, which is nearly 100% if the reflectance of aluminum is ignored. The coupling efficiency does not change even with ±1.5° angular deviation from 45°. Thin film VCSEL and PIN photodiodes are integrated on a flexible optical waveguide film.

Thermal management of the embedded VCSEL is the critical concern to insure its reliable operation. We investigated an effective heat sink structure for VCSEL. The 30μm thick copper film on the back side of VCSEL array turns out to be an excellent heat sink without the sacrificing the strategy of easy packaging. The authors would like to thank Chulchae Choi, Lei Lin and Yujie Liu who are previous PhD students participated in this program at UT, Austin.

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