Active transmission control based on photonic-crystal MOS capacitor

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ABSTRACT

Silicon nanophotonics has recently attracted great attention since it offers an opportunity for low cost opto-electronic solutions based on silicon complementary metal oxide semiconductor (MOS) technology. Photonic crystal (PhC) structures with slow photon effect are expected to play a key role in future large-scale ultra-compact photonic integrated circuits. A novel vertical-MOS-capacitor-based silicon PhC waveguide structure was proposed to achieve active transmission control via the free carrier plasma dispersion effect. We designed and fabricated a single-arm PhC waveguide with MOS gate defect using silicon-on-insulator (SOI) substrate and demonstrated that a defect mode was present in the infrared region. Plane wave expansion (PWE) method based simulation indicated that high group index of the fabricated PhC waveguide could be achieved near the transmission band edge. Further investigation demonstrated that such PhC MOS capacitor would be a good candidate to realize ultra-compact transmission control.

Keywords: Photonic crystal (PhC), metal oxide semiconductor (MOS) capacitor, Mach-Zehnder interferometers (MZI), silicon-on-insulator (SOI), plasma dispersion effect

I. INTRODUCTION

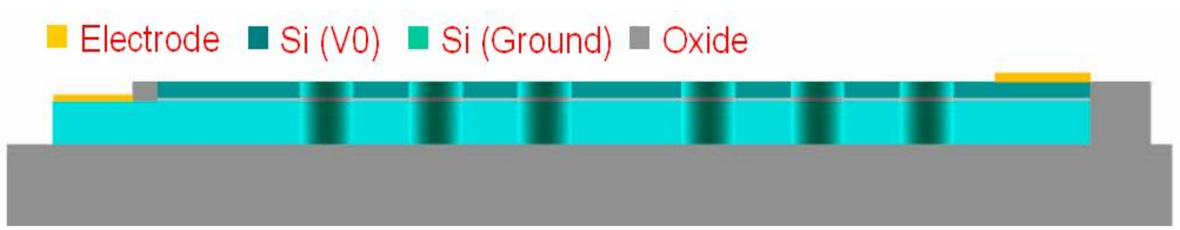
The beginning of 21st century witnesses the pervasive presence of nanostructures and nanofabrication in science and technology. In photonics, nanoscale structures, particularly photonic crystals [1-17], hold the promise of achieving optical functions in a significantly reduced device size with reduced power consumption (e.g. thresholdless lasers based on photonic crystal cavities [1]). Photonic crystals are a new class of materials that provide novel capabilities for the control and manipulation of light [1-3]. These materials have a period lattice formed from dielectric materials. An example is a single slab of semiconductor (high-dielectric) containing a periodic array of air-holes, which forms a two-dimensional (2D) photonic crystal. Optical waveguides based on photonic crystal line defects [4-6], the so-called photonic crystal waveguides (PCWs), have been demonstrated to provide five orders of magnitude larger dispersion than conventional dispersion compensating fiber. Such an extraordinary dispersion capability has a

Photonic Crystal Materials and Devices VI, edited by Ali Adibi, Shawn-Yu Lin, Axel Scherer,
Proc. of SPIE Vol. 6480, 64800W, (2007) · 0277-786X/07/$18 · doi: 10.1117/12.705613

profound impact on the phase change over a segment of photonic crystal waveguides. When incorporated in silicon Mach-Zehnder modulators, photonic crystal waveguides lead to a significant enhancement of modulation efficiency, which in turn allows us to reduce the modulator electrode length by several orders of magnitude.

Silicon optical modulators have been studied for almost two decades. Kerr effect, Franz-Keldysh effect, and plasma dispersion effect are the main mechanisms for modulating the refractive index of silicon. It has been long established that the former two effects have relatively low modulation efficiency [18], leaving the plasma dispersion effect the prime choice. For the plasma dispersion effect, free charge carriers are injected into silicon or induced in silicon through biased electrodes; and the refractive index changes with the increased carrier concentration in silicon. Capacitive coupling through the MOS field effect [19] and carrier injection by p-i-n diode structure [20] have been demonstrated as two practical methods to achieve active modulation of the free carriers in silicon. In this paper, we propose a novel MOS-capacitor-based silicon PhC waveguide structure and compare the horizontal and vertical MOS configurations in detail, including electrode design, capacitance and resistance evaluation, fabrication analysis and estimation of electrical and optical performance.

II. ACTIVE SILICON PHOTONIC CRYSTAL WAVEGUIDES INCORPORATING A MOS CAPACITOR



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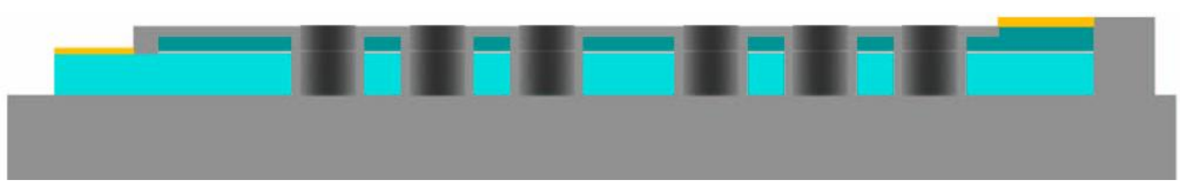

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Fig. 1. Schematic cross section of our horizontal MOS capacitor based PhC modulator design. The top Si (V0) layer is connected with high-frequency driving signal. The bottom layer is the buried oxide layer of the SOI wafer. (a) Before oxidation (b) After oxidation

Recently Intel have experimentally demonstrated 10-Ghz charge density modulation based on the MOS capacitor structure [21]. However, the Mach-Zehnder modulator is based on conventional rib waveguides, which usually need several millimeters to achieve the required phase shift between the signal and reference arms due to the fairly low propagation constant perturbation. In order to greatly reduce the total length of the modulator device, we combined such effect with photonic crystal theory to create an ultra-compact modulation device with high modulation frequency. We designed both horizontal and vertical MOS capacitor structures, compared the pros and cons of fabrication technique and evaluated the electrical and optical performances. Finally we chose the vertical layout as our first plan.

We have several basic design requirements for MOS-based Mach-Zehnder modulator device. First it is necessary to avoid multimode structure such that perfect interference can be achieved at the Y-junction part. And metal contact should be prevented within the core region to reduce the additional propagation loss caused by metal absorption. Considering the electrical performance, we need to realize practical connection with peripheral circuits.

Figure 1 shows the PhC cross section of our horizontal layout before and after oxidation process. SOI wafer consisted of the single-crystal Si (aqua) and buried oxide (gray) layers. The gate oxide (gray) and top poly-silicon (bottle green) layers would be fabricated by gate oxidation and poly-silicon deposition. We did not plan to custom design a multi-insulator-layer SOI wafer fabricated by oxygen implantation since the buried oxide thickness limit for SOI wafer was always larger than 150 nm while the expected thickness of the gate oxide layer was smaller than 100 nm. The six apertures in each schematic illustrate the air holes of the PCW with the core region in the center. We designed post oxidation to effectively avoid short circuit between driving signal and ground layers. Post oxidation could etch away part of the silicon sidewall and form an oxide insulation layer. The etching speed depends on the surface roughness during oxidation such that the quality of the sidewall surface can be improved evidently.

The predominance of horizontal gate oxide design is the large active modulation region due to the oblate cross section (0.7 x 0.24 μm) of the PCW core region. Conventional fabrication process for horizontal configuration can be applied to form very thin gate oxide layer, which is required to reduce the device driving voltage. However, a balance exists between the optical propagation loss and the thickness of the poly-silicon layer. The top poly-silicon layer with high doping concentration would cause huge additional insertion loss, while an ultra-thin poly-silicon layer would greatly increase the silicon resistance and modulation frequency would be limited because the horizontal MOS structure is capacitive. The optical propagation loss can be partially reduced with patterned poly-silicon layer which is only covering the active photonic crystal region. Furthermore, complex electrode design was inevitable since strong vertical electric field was necessary for the free carrier plasma dispersion effect whereas simple electrode design only induced strong horizontal electric field. Thus, we shifted our focus to vertical layout design.

Figure 2 illustrates the cross section of the vertical layout design. Normal SOI wafers were used as the substrate. The Si layer (aqua) was implanted as p^- region and connected with aluminum electrodes via ohm contacts. High-voltage RF signal drove the MOS capacitor structure and generated necessary electric field for charge density modulation. Under accumulation conditions, the majority carriers in the Si layer modified the refractive index and induced large phase shift in the defect mode due to the high dispersion character of photonic crystals.

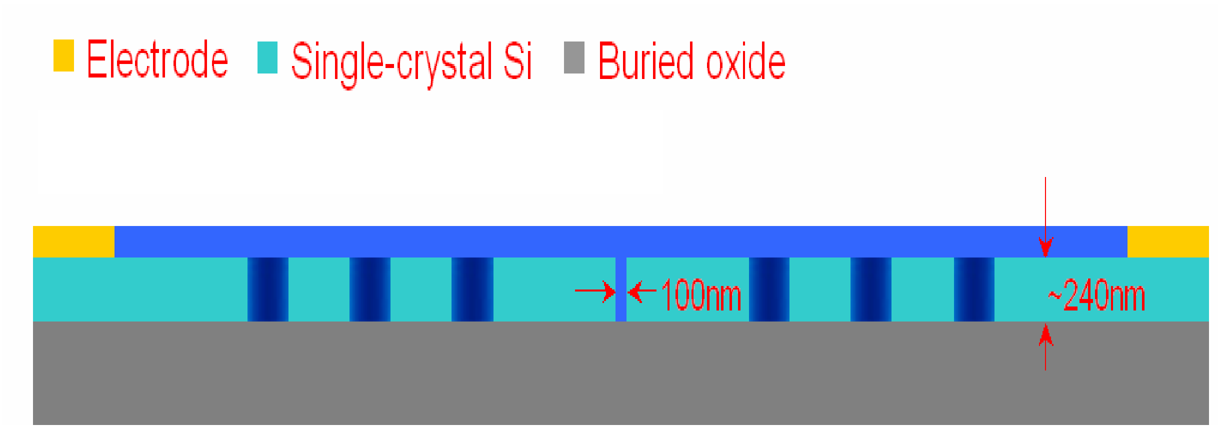
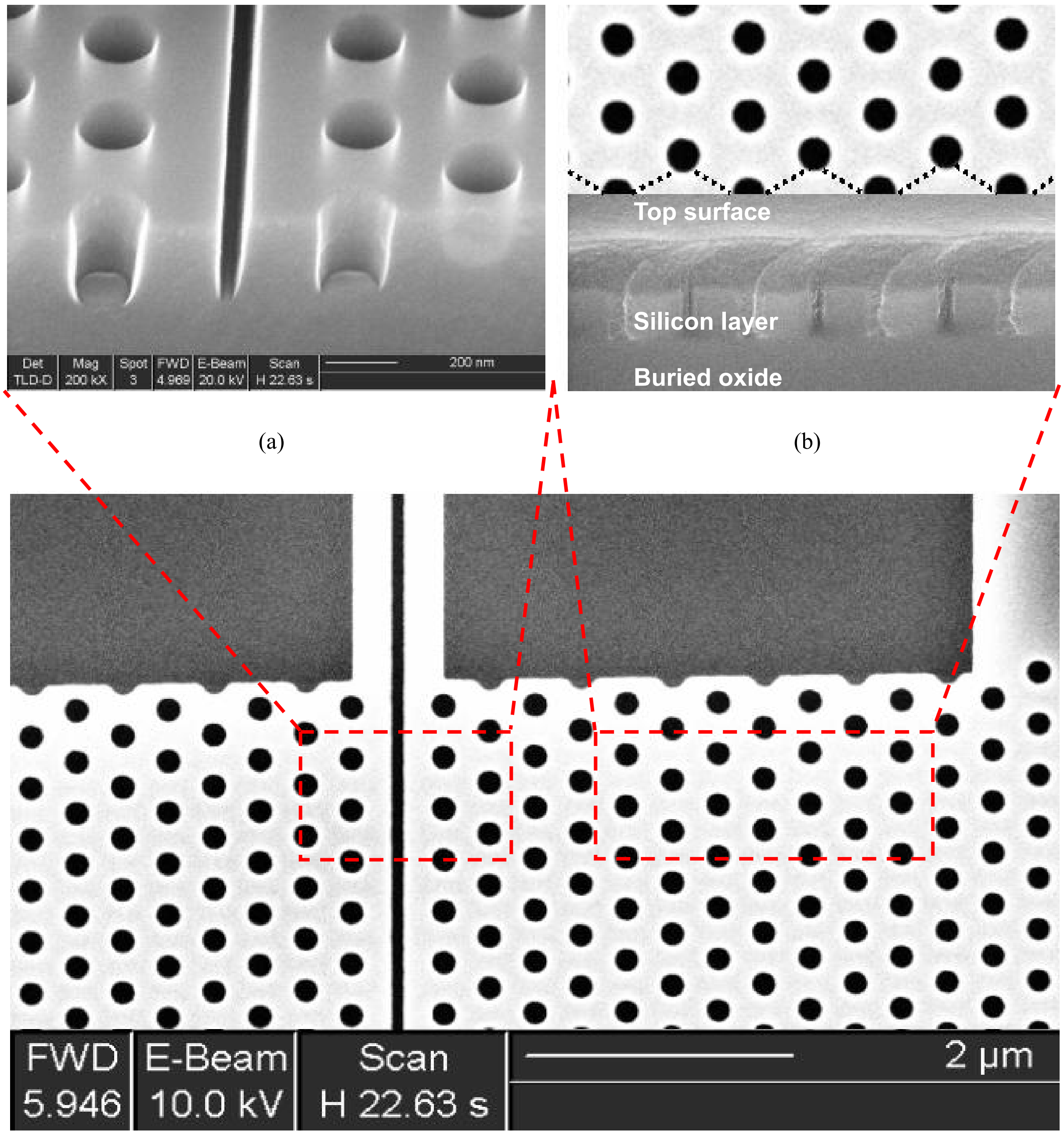


Fig. 2. Schematic cross section of our vertical MOS capacitor based PhC modulator design.

The air holes and vertical MOS gate trench were fabricated via E-beam lithography and standard reactive ion etch (RIE). The 0.1 x 0.24-µm cross-section caused the gate aspect ratio larger than 2. The SEM micrograph in Fig. 3 (a) confirmed conventional RIE technique could achieve such aspect ratio via precise calibration. Then we needed to fill in the center trench to generate the vertical MOS gate with high breakdown strength. High-density plasma chemical vapor deposition (HDPCVD) techniques could be applied to fill in the narrow slot with aspect ratio larger than 2. Fig. 3 (b) illustrates the filling performance. We cleaved the filled sample using our scribing machine, in order to scan the cross section of the PhC region. The broken line in Fig. 3 (b) shows the split path after cleaving.



(c)

Fig. 3. SEM micrographs of PCW with vertical MOS gate.

III. Optical characteristic optimization and measurement result

Measurement shows the coupling efficiency between conventional channel waveguide and slot waveguide is very low since slot waveguide confines light inside the center trench region [22]. The lower pictures in Fig. 4 illustrate the mode profiles of channel waveguide and slot waveguide respectively. In order to improve the coupling efficiency and achieve high enough output light power, we optimized the slot waveguide and photonic crystal waveguide and designed a multi-mode interference (MMI) coupling structure to prevent the mode profile mismatch.

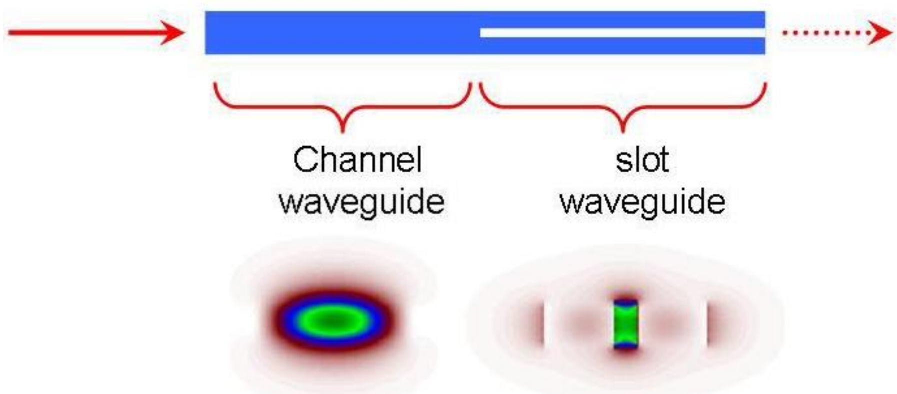
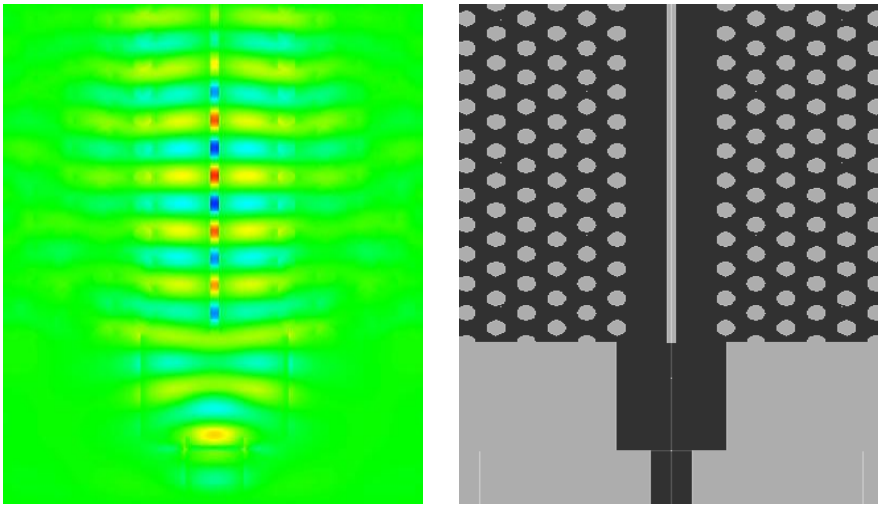


Fig. 4. Coupling efficiency measurement and mode profile comparison.

We applied 3D FDTD simulation to evaluate the coupling performance. Fig. 5 (a) shows the top view of the intensity distribution and the MMI coupling structure between channel waveguide and PhC waveguide with center trench. The defect width of PhC waveguide is enlarged to match the mode profile. Measurement shows the coupling efficiency has been improved to 70% with MMI coupling structure applied. Plane-wave expansion (PWE) method is applied to calculate the band structure of the PhC waveguide as shown in Fig. 5 (b). The defect mode part is zoomed in and matched with the measured transmission spectrum based on normalized frequency. Simulation indicates that high group index of the fabricated PhC waveguide can be achieved near the transmission band edge. The induced slow photon effect has been demonstrated as a practical approach to greatly reduce the total length of the active region [20, 23]. Our further investigation on static modulation test indicated sufficient phase shift caused by plasma dispersion effect could be achieved.



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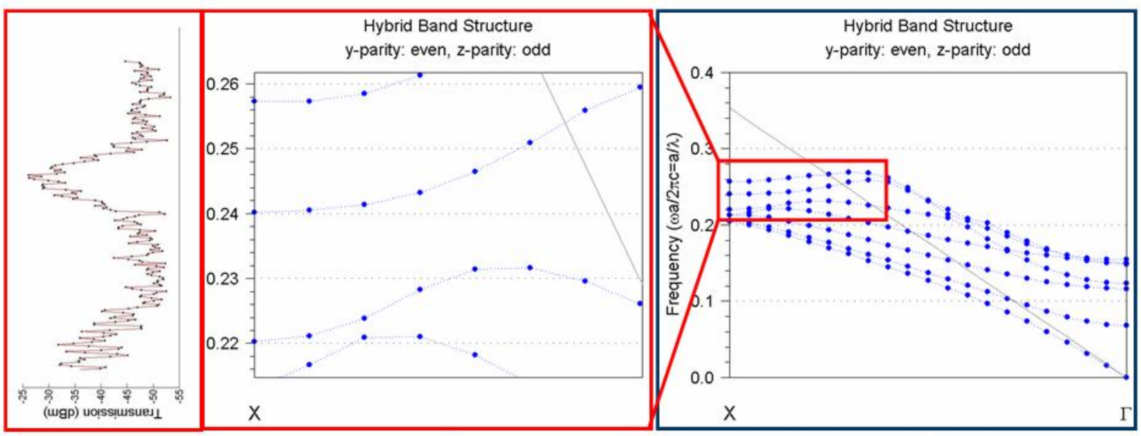

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Fig. 5. (a) Intensity distribution of MMI coupling structure between conventional channel waveguide and photonic crystal waveguide with center trench. (b) Simulated band structure and measured transmission spectrum of PhC waveguide.

IV. CONCLUSION

PhC MOS capacitor based ultra compact active transmission controllers operating at communication wavelength (1550nm) have been investigated. The horizontal and vertical MOS structures have been designed and evaluated based on electrical and optical performance. Vertical MOS structures have been chosen as our first choice and fabricated on SOI wafers. We have further optimized the coupling structure and simulated the optical characteristics of PCW. Spectrum measurement indicated that a defect mode was present in the infrared region. The high group index of PCW and low capacitive character of vertical MOS structure demonstrated that such PhC MOS capacitor would be a good candidate to realize ultra-compact high-speed transmission control.

ACKNOWLEDGMENTS

This research is supported in part by AFOSR and DARPA. The devices were fabricated at UT MRC with nanofabrication facilities partially supported under NSF's NNIN program. We thank the CNM of UT Austin, Welch Foundation and SPRING for partial support of the Dual Beam FIB/SEM usage.

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